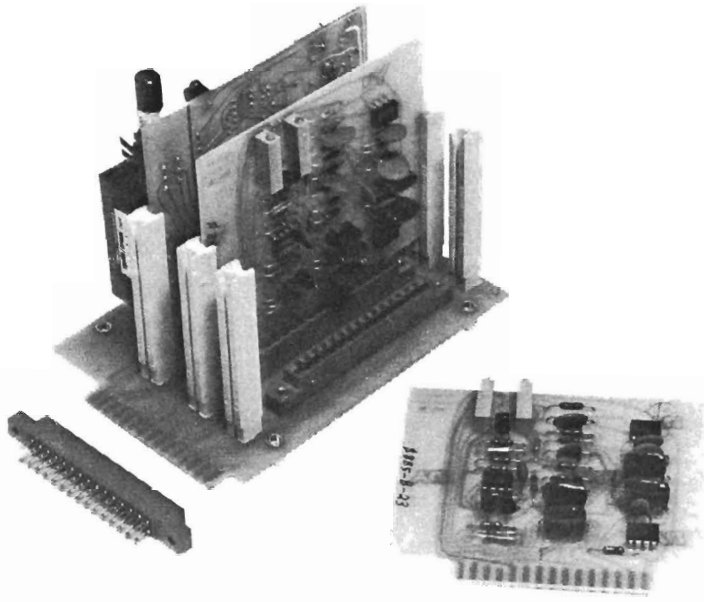
CD72-2 / CD72-4
Multichannel
Carrier Demodulators

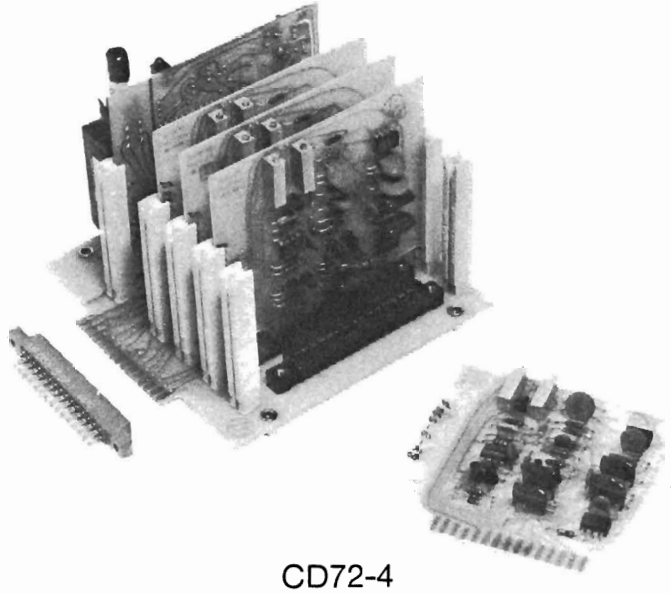
TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

LIST OF TABLES



CD72-2



CD72-4

FIGURE 1-1. Model CD72 Configurations

SECTION I
DESCRIPTION

1-1. DESCRIPTION

The CD72 Carrier Demodulator supplies carrier excitation to variable reluctance transducers and provides two (CD72-2) or four (CD72-4) independent channels of transducer signal conditioning to an output signal level of ±10 Vdc full scale.

1-2. The CD72 consists of circuit boards which plug into an interconnecting mother board. One circuit board is the oscillator power supply, which supplies 5 Vrms 5 kHz carrier excitation and ±15 Vdc power to the carrier demodulator boards. Each carrier demodulator board has a screwdriver adjusted ZERO control and SPAN control. The demodulated output from each channel is ±10 Vdc when operating with a transducer whose full scale output sensitivity is at least 17 mV/V. The dc output is a low noise, low impedance signal which may be used to drive meters, oscillographs, galvanometers, strip chart recorders, oscilloscopes or other indicating devices for static or dynamic measurements.

1-3. The CD72 is designed for OEM applications in dedicated installations requiring modular multichannel capability at low cost. Although intended for use with half-bridge variable reluctance transducers, the CD72 can also be used with LVDT, RVDT or potentiometric transducers.

1-4. TECHNICAL CHARACTERISTICS

The Technical Characteristics for the CD72 are listed in Table 1-1.

1-5. PHYSICAL CONFIGURATION

Outline drawings for the CD72-2 and CD72-4 are included in the Appendix.

TABLE 1-1. Technical Characteristics

Item	Characteristics
Oscillator Power Supply	
Carrier:	5 Vrms, 5 kHz ±1%
DC Power:	±15 Vdc
Input Power:	95 to 125 Vac, 50 to 400 Hz, 3 VA
Demodulator (Typical, each channel)	
Input Sensitivity:	17 mV/V, min. for 10 Vdc output
Maximum Input:	2.5 Vrms, 5 kHz
Span Control:	0 to 100% FS
Zero Control:	±10 mV/V
Bridge Excitation:	5 Vrms, 5 kHz
Output:	0 to ±10 Vdc, 10 mA into 1 kΩ load, short-circuit protected
Output Impedance:	10 Ω, nominal
Output Ripple:	10 mV pk-pk, maximum
Linearity:	0.05% FS, maximum
Long Term Stability	0.1% FS
Frequency Response:	Flat ±5%, 0 to 1000 Hz
Temperature Range:	0° to + 185°F
Thermal Zero Shift:	0.005% FS/°F
Thermal Span Shift:	0.01% FS/°F

SECTION II
INSTALLATION AND OPERATION

2-1. INSTALLATION

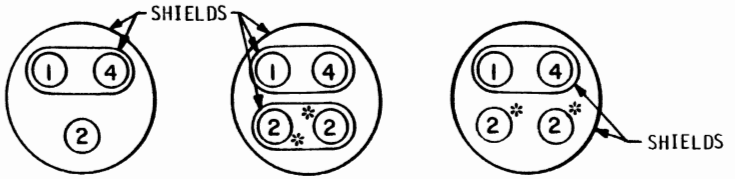
The CD72 may be installed in any orientation. If mounted in an unvented enclosure, there must be adequate ventilation to keep the ambient temperature below 185°F. Four threaded standoff's are provided on the mother board for mounting (See Outline Drawings for size and locations).

2-2. Wiring between the CD72 and the transducers may be unshielded if the run is 3 feet for less. For longer runs, a three or four conductor shielded cable should be used. A cable with multiple shielded pairs may be used if the transducer excitation leads (transducer Pins 1 and 4) are connected in one pair and the signal lead(s) connected to another shielded conductor or pair. If one excitation lead and the transducer output lead are connected in one shielded pair and the other excitation lead run by some other means, the capacitive unbalance may shift the transducer zero more than can be corrected by the demodulator ZERO control.

2-3. Figure 2-1 shows preferred and unacceptable cable types for long runs between the transducer and the CD72.

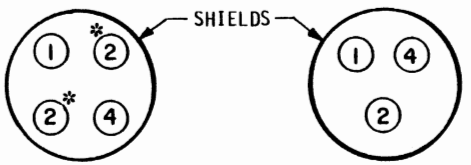
2-4. Figure 2-2 shows the typical fabrication of a transducer cable for use with most Validyne pressure transducers, which have WK-4-32S connectors.

2-5. The CD72 input power is controlled by a push-type ON-OFF switch mounted on the top right-hand side of the power supply circuit board. Mounted next to this switch is a LED indicator light which is lit when power is on. Figure 2-4 shows the location of the Power Supply Controls and Indicators.



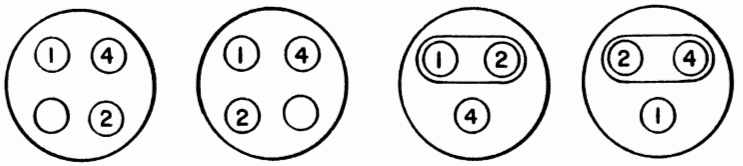
PREFERRED CABLE TYPES & ARRANGEMENTS

(Lengths to 1,000 ft. or more)



ACCEPTABLE CABLE TYPES & ARRANGEMENTS

(Lengths to approx. 100 ft.)

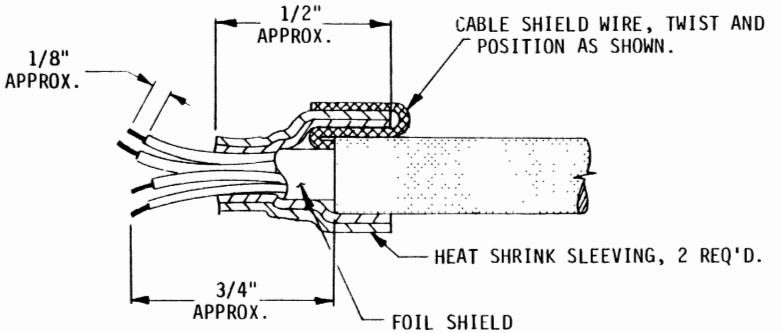


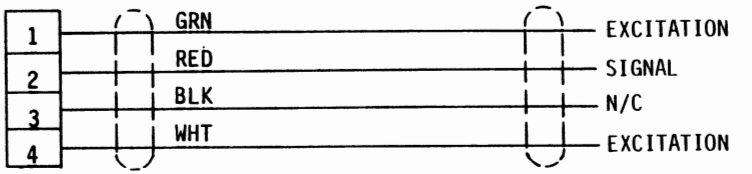
Unequal distance between signal lead and each carrier lead - capacitive unbalance

One carrier lead and signal lead in common shield - large capacitive unbalance

NOT RECOMMENDED

FIGURE 2-1. TRANSDUCER CABLING





NOTES:

1. Leads for pins 1 and 4 should be in one shielded pair; signal leads 2 and 3 in the other shielded pair (provided two pairs are used).

FIGURE 2-2. CABLE FABRICATION

2-6. NOTE: The power switch has a set of single-pole single-throw contacts available for closing an external circuit when CD72 power is on. See Figure 5-1, Appendix. Connections to this switch circuit must be made at terminals 6 and 7 of the power supply circuit board connector; these switch terminals are not available at the mother board input/output connector.

2-7. INPUT AND OUTPUT CONNECTIONS

Input and output connections to the CD72 are made by means of a printed circuit board edge connector which plugs into the mother board.

NOTE: PIN CONNECTIONS ARE DIFFERENT FOR THE CD72-2 vs CD72-4

The pin connections to the mother board are as follows:

2-8. CD72-2: The CD72-2 uses a single row (15 contact) connector with pierced eyelet terminals.

Terminal No.	Function	
1	115 Vac (high side of line)	Power Input
2	115 Vac (low side of line)	
3	AC Line Ground pin (Guard)	
4	N/C	
5	Carrier Excitation, Transducer pin 4	Channel "A"
6	Input, Transducer pin 2	
7	Carrier Excitation, Transducer pin 1	
8	Carrier Excitation, Transducer pin 4	Channel "B"
9	Input, Transducer pin 2	
10	Carrier Excitation, Transducer pin 1	
11	Output Common, Signal Ground	
12	Output "A"	
13	Output "B"	
14	N/C	
15	N/C	

If the connector is plugged in upside down, the 115 V power will be connected to unused pins and no damage will be done to the unit.

2-9. CD72-4: The CD72-4 uses a dual row (15 contacts per row) connector with pierced eyelet terminals.

CAUTION: IF THE CONNECTOR IS PLUGGED IN UPSIDE DOWN, THE 115 V LINE WILL CAUSE SEVERE DAMAGE.

Function	Terminal No. Side A	Terminal No. Side B	Function
115 Vac (High Side of Line)	1	A	115 Vac (High Side of Line)
115 Vac (Low Side of Line)	2	B	115 Vac (Low Side of Line)
AC Line Ground (Guard)	3	C	AC Line Ground (Guard)
N/C	4	D	N/C
-15 Vdc	5	E	Circuit Ground
+15 Vdc	6	F	N/C
Output "A"	7	G	Output "C"
Signal Ground	8	J	Signal Ground
Output "B"	9	k	Output"D"
Channel "A" Excitation (Pin 4)*	10	L	Excitation (Pin 4)* Channel "C"
Channel "A" Excitation (Pin 1)*	11	M	Excitation (Pin 1)* Channel "C"
Channel "A" Input "A" (Pin 2)*	12	N	Input "C" (Pin 2)* Channel "C"
Channel "B" Excitation (Pin 4)*	13	P	Excitation (Pin 4)* Channel "D"
Channel "B" Excitation (Pin 1)*	14	R	Excitation (Pin 1)* Channel "D"
Channel "B" Input "B" (Pin 2)*	15	S	Input "D" (Pin 2)* Channel "D"

NOTES: 1. Side A is component side of board, Side B is solder side.
*2. Pin numbers referred to are transducer connector pins.

2-10. OPERATION (Reference Figures 2-3 and 2-4)

The following procedures cover the operational setup of each channel for variable reluctance inputs:

A. Connect the transducers per Paragraph 2-7, Input/Output Connections. Connect a DC digital voltmeter to the Output and Output Common terminals. Turn CD72 power on.

2-10. OPERATION (Cont'd)

B. Apply zero stimulus to the transducer and adjust the screwdriver ZERO control for a DVM reading of 0.000 ±0.005 Vdc.

C. Apply full scale stimulus to the transducer and adjust the screwdriver SPAN control for a DVM reading of 10 Vdc or the desired full scale output signal. If the output voltage polarity is opposite of the desired polarity, reverse the transducer carrier leads at the input connections.

D. Recheck the zero output and readjust, if necessary.

E. Repeat steps A through D for each transducer to be connected.

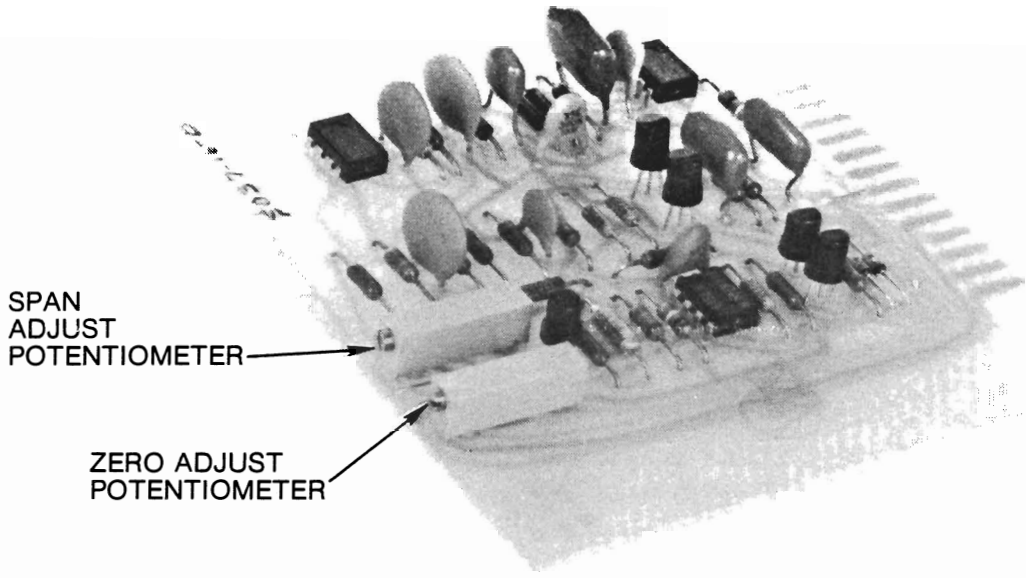


FIGURE 2-3. Plug-in Carrier Demodulator Board

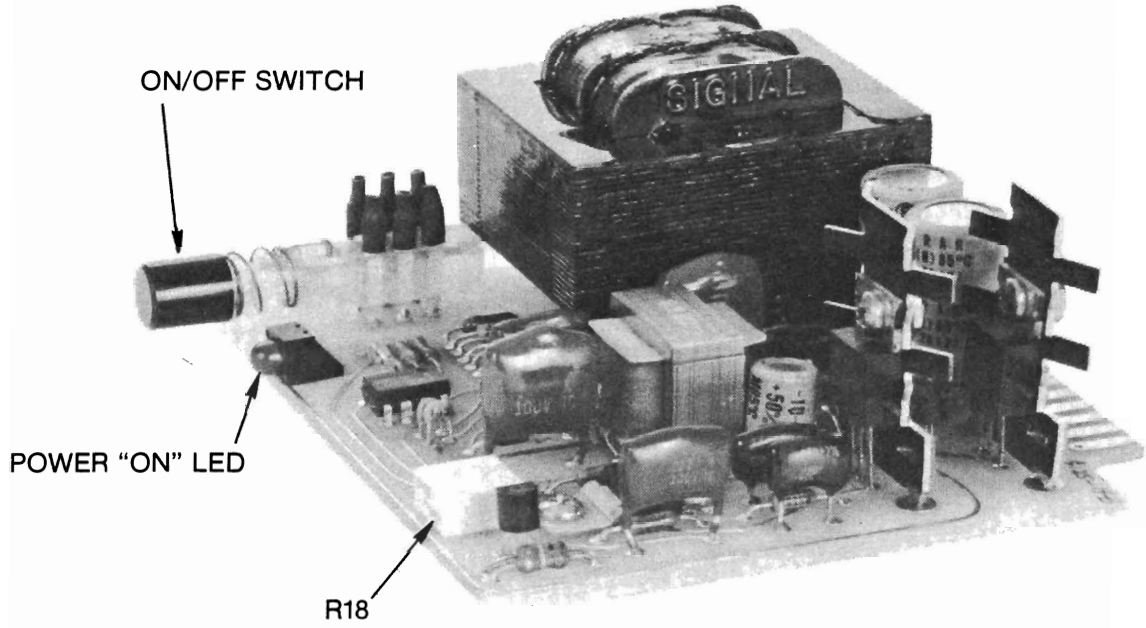


FIGURE 2-4. Plug-in Power Supply Board

SECTION III
PRINCIPLES OF OPERATION

3-1. OSCILLATOR POWER SUPPLY (Reference Figure 5-1, Appendix)

The AC input power is reduced and rectified by transformer T1 and diode bridge CR2. Voltage regulators U1 and U2 fix the DC voltages at +15 Vdc and -15 Vdc. This ±15 Vdc operates the carrier oscillator circuit and is fed by the mother board to all carrier demodulator positions.

3-2. The carrier oscillator is a voltage-stabilized Wien bridge circuit which supplies carrier excitation to all module positions thru center-tapped transformer T2. C12, R12, C13, and R17 form the positive feedback frequency determining network. R13, R11 and field effect transistor Q2 form the opposing negative feedback loop. When the negative feedback is equal to the positive feedback, the amplitude of oscillation is stable. The amount of negative feedback is controlled by the resistance of Q2, which depends on its DC gate voltage.

3-3. U3 is a fast acting DC integrator whose output controls the gate voltage of Q2. The input to integrator U3 is a negative voltage from reference zener diode CR9 and a positive voltage from the carrier amplitude detector circuit. If the carrier amplitude is low, the positive voltage from the amplitude detector will be less than the negative voltage from the reference zener. This will cause the integrator output to decrease the negative feedback thus increasing the carrier amplitude. If the carrier is too large, the integrator output changes in the opposite manner, again restoring the carrier amplitude.

3-4. The carrier amplitude detector circuit is comprised of CR5, CR6, CR7 and CR8. These rectify the carrier to provide an integrator input proportional to the average carrier amplitude. This control circuit, operating from the secondary of the transducer excitation transformer (T2), makes the carrier amplitude virtually independent of loading and controlled almost entirely by the very stable reference zener diode CR9.

3-5. CARRIER DEMODULATOR (Reference Figure 5-2, Appendix)

The transducer is excited from a transformer with a precision grounded center tap. The unbalance of the transducer coils is then seen as an AC voltage with respect to signal ground (Pin 5 on demodulator circuit card). This signal, a function of the stimulus on the transducer, is fed through Q201, a unity gain buffer amplifier. At this point, it is summed with a signal from the ZERO control. This allows any residual output at zero pressure to be nulled.

3-6. The transducer signal then goes to the SPAN potentiometer and then to the AC amplifier, U201. The output of U201 is directed alternately into the inverting and noninverting inputs of DC amplifier U202 by demodulator transistors, Q202 and Q203. These transistors are controlled by carrier zero-crossing detectors Q204 and Q205. For positive pressure the AC ouput of U201 is positive when Q203 is nonconducting, allowing the positive signal to enter the noninverting input of U202, thus producing a positive output. On the next half of the AC cycle, when the output of U201 is negative, U202 is nonconducting allowing the negative signal to enter the inverting input of U202 again producing a positive DC output. This results in a synchronously demodulated signal at the output of U202. The carrier ripple present in the DC output is partly filtered by U202. The DC output of U202 is further filtered by U203, a unity gain, 3-pole low pass filter. This stage provides a low noise, low impedance output signal with excellent static and dynamic response.

SECTION IV
MAINTENANCE AND REPAIR

4-1. MAINTENANCE

If a periodic maintenance test schedule is in effect, the following procedures can be used to verify that the CD72 is properly operational. For these tests the following equipment is required: Validyne Model TS234 Transducer Simulator and an AC/DC Digital Voltmeter. See Paragraph 2-7 for input/output terminal identification.

A. Connect an AC DVM to the carrier excitation terminals of Channel A. Turn CD72 power on. The DVM should read 5.00 ±0.05 Vrms. If not, use a small screwdriver to adjust R18 (at the top front of the power supply circuit board -- see Figure 2-4 for location) for a carrier voltage of 5.00 ±0.05 Vrms. If desired an oscilloscope can be used to check the 5 kHz wave form, which should be sinusoidal.

B. Remove the carrier demodulator board from the Channel A position. Connect a DC DVM with test probes to terminal 15 (+) and 5 (COM) of the circuit board connector on the mother board. The DVM reading should be +15.0 ±0.6 Vdc.

C. Connect the test probes to terminal 7 (-) and 5 (COM) of the circuit board connector. The DVM reading should be -15.0 ±0.6 Vdc.

D. The above procedures check the carrier excitation and DC operating voltage levels supplied to all signal conditioning modules.

E. Connect the TS234 Transducer Simulator to Channel A as follows:

TS234		CD72-2	or	CD72-4
Terminal 1	to	Terminal 7		Terminal 11
Terminal 2	to	Terminal 6		Terminal 12
Terminal 4	to	Terminal 5		Terminal 10

Connect the DVM to terminal 12 (+) and terminal 11 (Gnd) of the CD72-2 mother board, or pins 7 (+) and 8 (Gnd) of the CD72-4 mother board.

F. Set the TS234 output switch to 0% and adjust the Channel A ZERO control for a DVM reading of 0.000 ±0.005 Vdc.

G. Set the TS234 switch to 100%, the polarity switch to +, and adjust the RANGE dial for a TS234 output of 17 mV/V (a dial setting of (170). Adjust the Channel A SPAN control for a DVM reading of 10.000 ±0.005 Vdc.

H. Set the TS234 switch to 50%. The DVM should read 50% of the output span within ±0.01 Vdc.

J. The above procedures check the input sensitivity, Zero adjustment, Span adjustment, and linearity of the Channel A carrier demodulator. If these adjustments cannot be made, the module should be set aside for repair or replacement.

K. Repeat Steps E thru H for each channel of the CD72.

4-2. REPAIR

The CD72 is tested, burned-in and retested before shipment to assure reliability and long life. Should malfunction occur, Validyne recommends that the defective module be returned to the factory for prompt repair or replacement in accordance with the Validyne warranty. For spare parts, order the following:

Validyne P/N 9617, CD72 Power Supply Board
Validyne P/N 7344-1, CD72 Carrier Demodulator Board

5-0. APPENDIX

This Section contains the following:

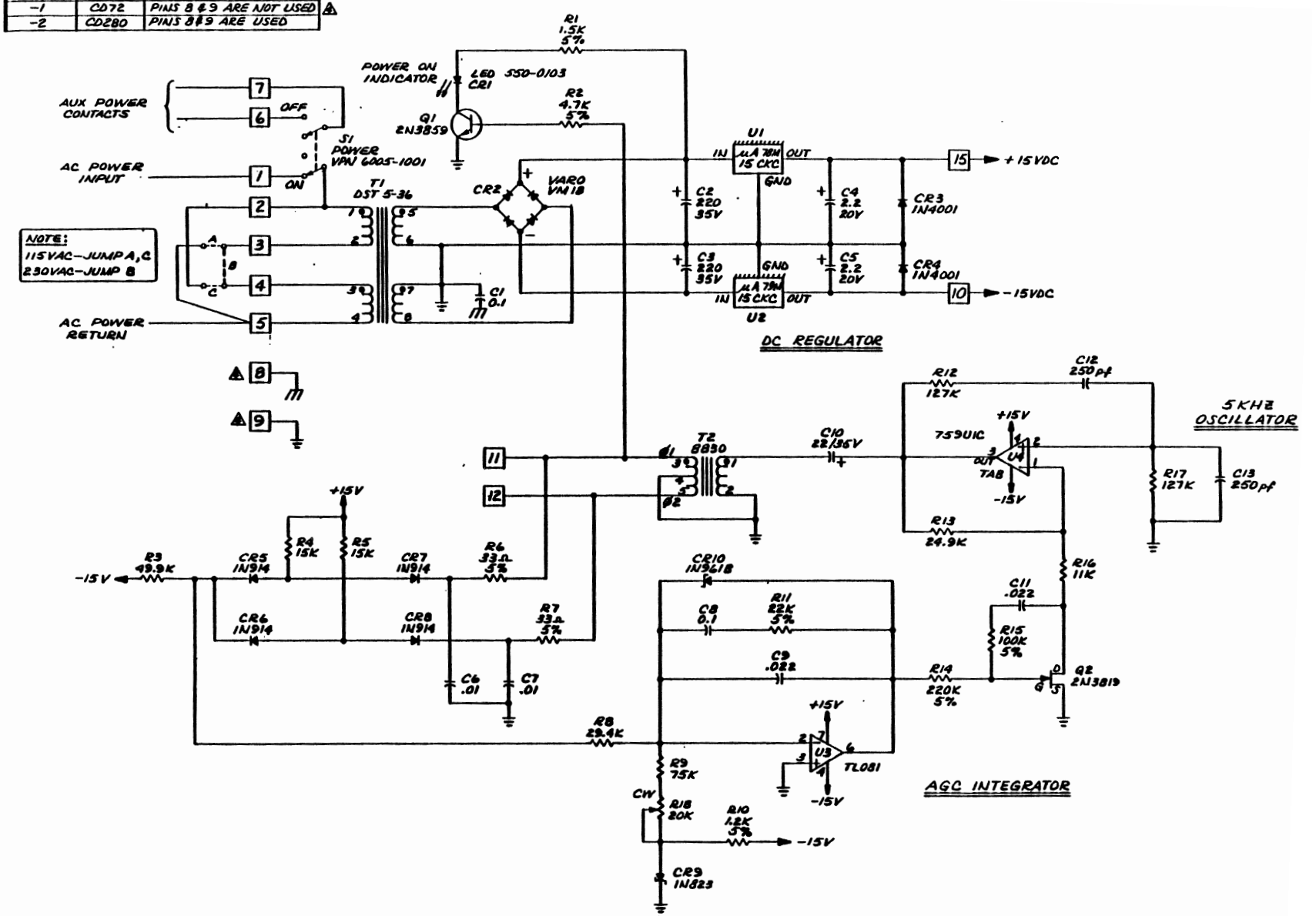
a) Figure 5-1. Oscillator Power Supply Schematic

b) Figure 5-2. Carrier Demodulator Schematic

c) Figure 5-3. Outline/Installation Drawing, CD72-2

d) Figure 5-4. Outline/Installation Drawing, CD72-4

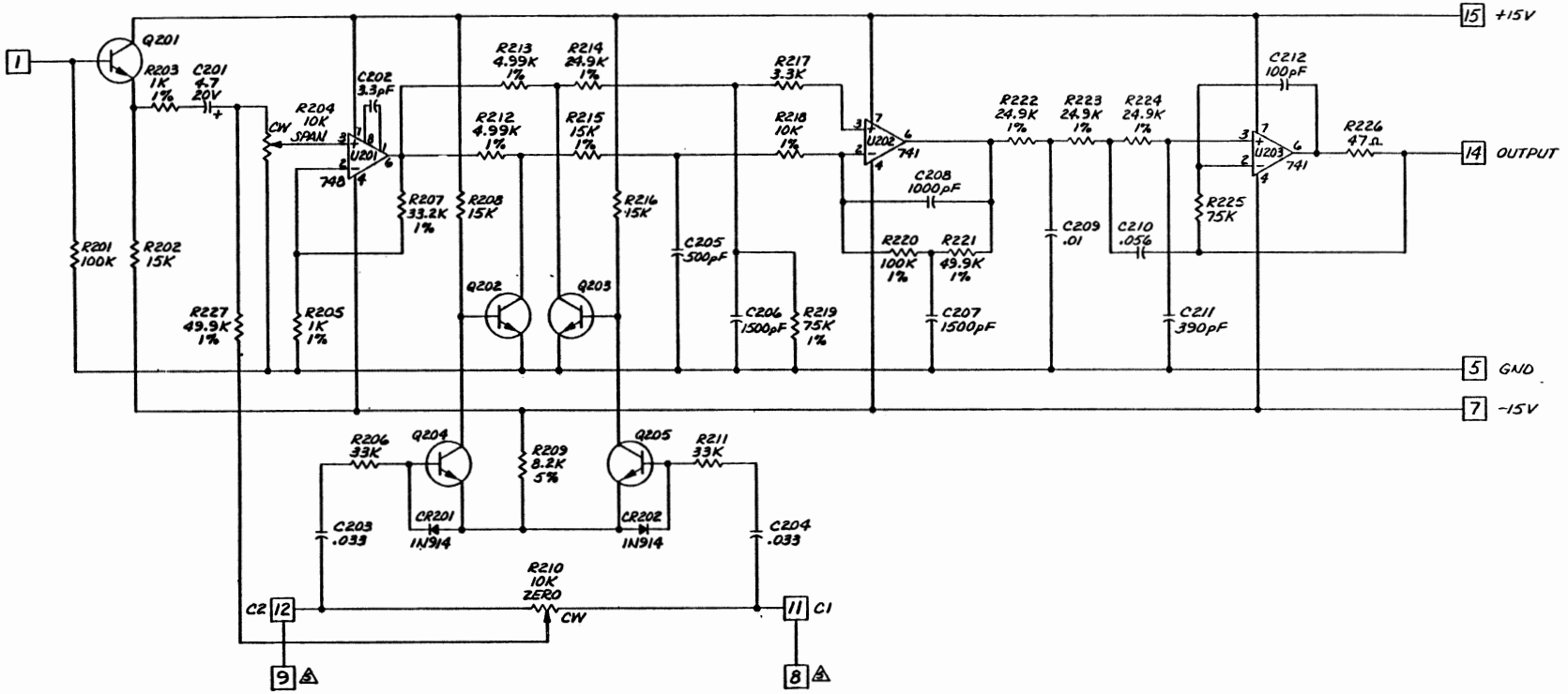
DASH NO.	MODEL	DESCRIPTION
-1	CD72	PINS 8 & 9 ARE NOT USED ⚠
-2	CD280	PINS 8 & 9 ARE USED



⚠ CONNECTOR PINS USED ON CD280 ONLY.
3. ☐ INDICATES TERMINALS ON CIRCUIT BOARD.
2. CAPACITOR VALUES ARE IN MICROFARADS.
1. RESISTOR VALUES ARE IN OHMS ±1%, ⅛ WATT.

NOTES: UNLESS OTHERWISE SPECIFIED.

FIGURE 5-1. Oscillator Power Supply Schematic



⚠ CONNECTOR PINS USED ON CD280 ONLY.
4. □ INDICATES CIRCUIT BOARD CONNECTOR PIN NUMBERS.
3. TRANSISTORS ARE 2N3859.
2. CAPACITOR VALUES ARE IN MICROFARADS.
1. RESISTOR VALUES ARE IN OHMS ±10%, ¼ WATT.
NOTES: UNLESS OTHERWISE SPECIFIED.

FIGURE 5-2. Carrier Demodulator Schematic

CD72-2

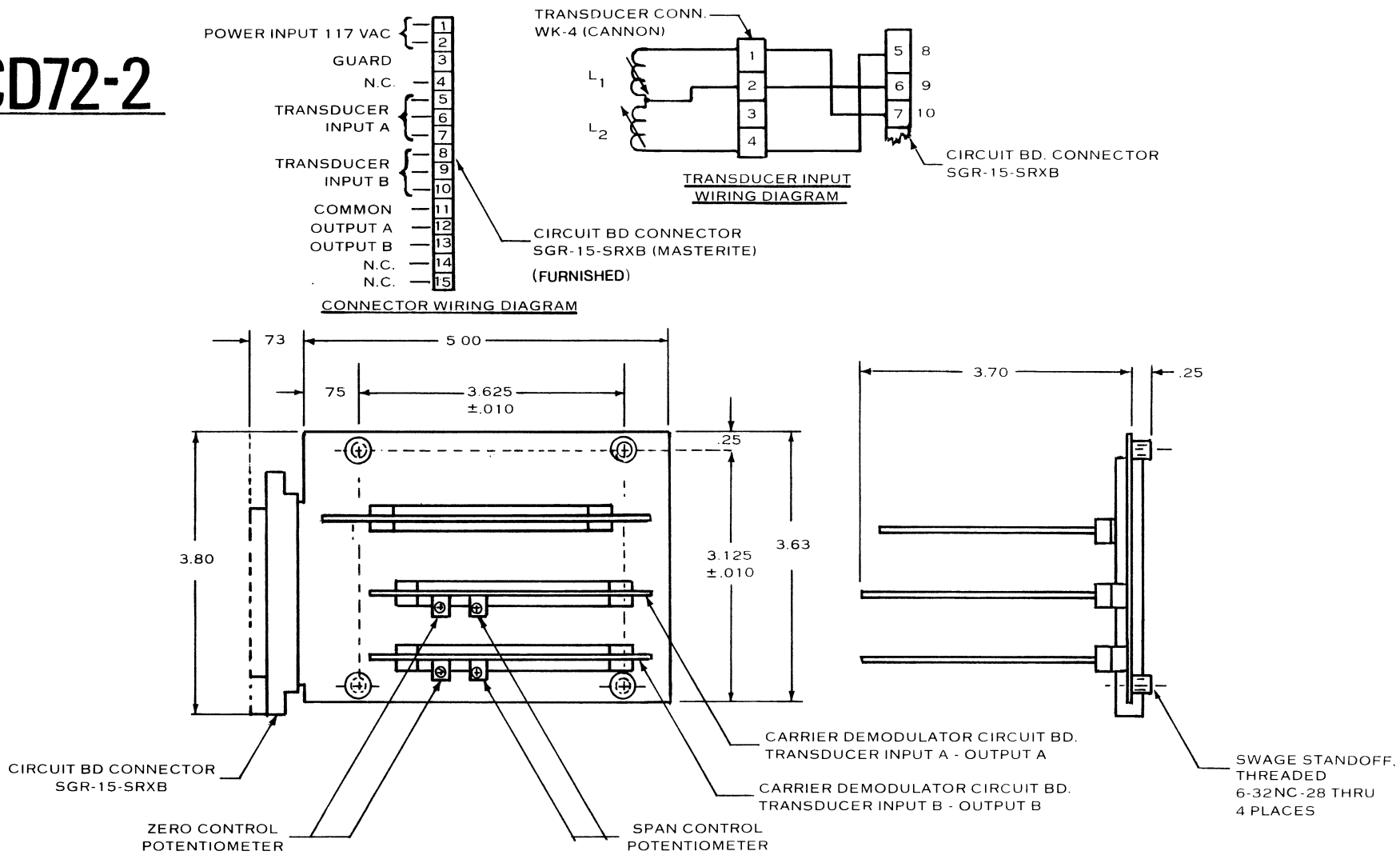
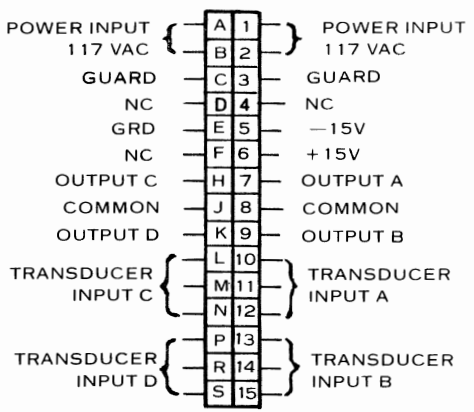
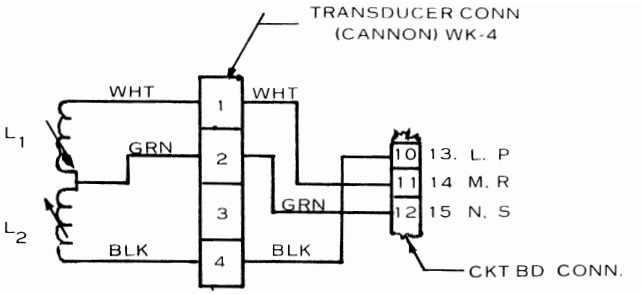


FIGURE 5-3. Outline/Installation Drawing, CD72-2

CD72-4



CONNECTOR WIRING DIAGRAM
CIRCUIT BD. CONNECTOR
00-6007-030-450-018 (ELCO)
(FURNISHED)



TRANSDUCER INPUT WIRING DIAGRAM

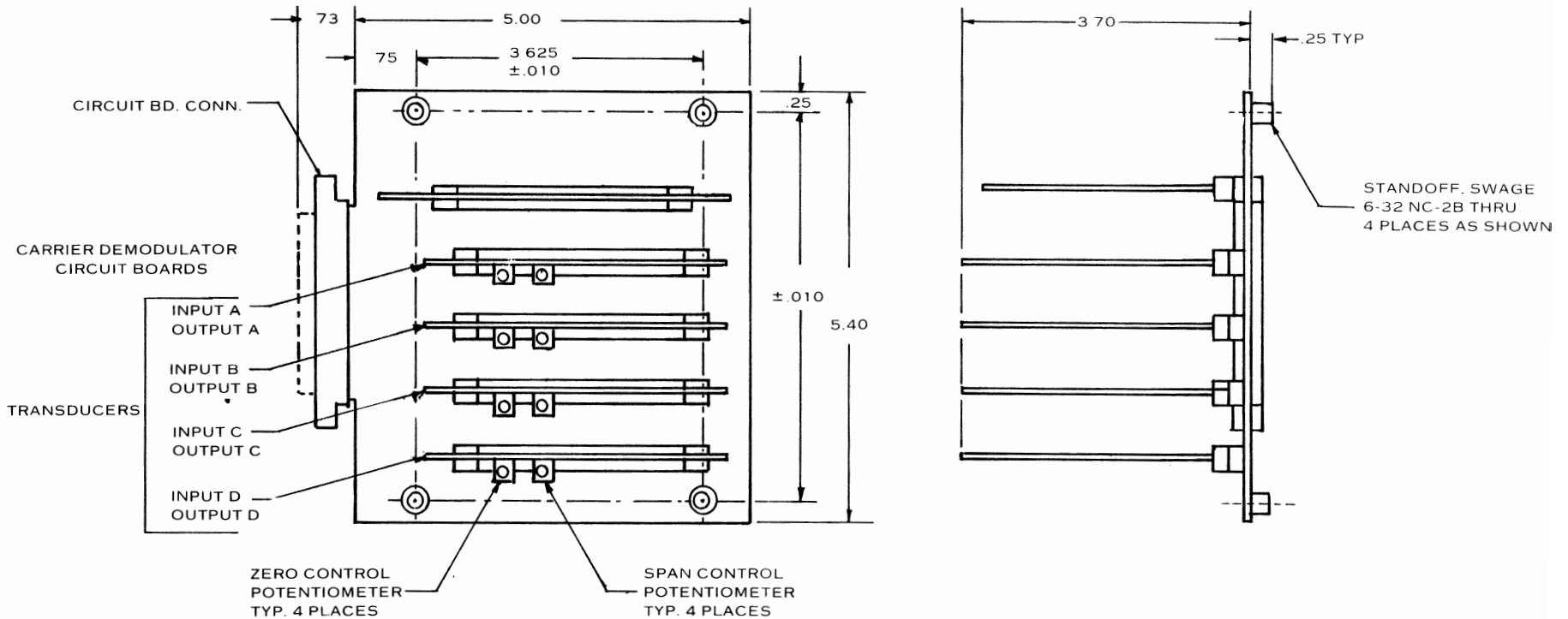


FIGURE 5-4. Outline/Installation Drawing, CD72-4