INSTRUCTION MANUAL

MR312-Q1

MASTER RECEIVER/ MODULE CASE

Including

DR317-X-Q1 Receiver Input Module

CS348-Q1 Control Sequencer Card

AG351-Q1 Address Generator Card

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Warranty coverage on repairs is 90 days on work done, or to the end of the original warranty period, whichever is longest.

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REVISION PAGE

DATE	PAGE NO.	DESCRIPTION OF CHANGE	BY

SECTION I
GENERAL DESCRIPTION

1-1. INTRODUCTION.

This technical manual contains operation and maintenance procedures for the MR312-Q1 Master Receiver, including the MR312-Q1 Module Case, DR317-Q1 Receiver Input Cards, CS348-Q1 Control Sequencer Card and the AG351-Q1 Address Generator Card. Other cards and modules which are part of the MR312-Q1 are covered in separate manuals. These include the DD354-Q1 Differential Driver Card, DR355-Q1 Differential Receiver Card, CI356-Q1 Computer Interface Card, PS320-Q1 Power Supply Module, TG319-Q1 Time Code Generator Module and optional RC321 Tape Control Module, and DD313-Q1 Digital-to-Analog Converter Module. The MR312-Q1 comprises a portion of the DA310 High Speed Data Acquisition System manufactured by Validyne Engineering Corporation, Northridge, California.

1-2. PURPOSE AND USE.

The MR312-Q1 Master Receiver is capable of receiving serial data directly from up to 16 MC170AD-Q2, MC370AD-Q2 or RM334 Remote Multiplexers, from up to 16 MX311-Q1 Digital Submultiplexers, or any combination thereof. Each input is hereinafter referred to as a "link". From each of the 16 input links, the Master Receiver can receive up to 256 data words simultaneously and store them in a random access memory (RAM) for controlled output into a computer.

1-3. The various link data can then be supplied by the MR312-Q1 to remote MC314-Q1 Digital-to-Analog Converter Module Cases which can contain either DA313-Q1 Digital-to-Analog converter (DAC) Modules or DD326-Q1 Digital Decoder Modules. Data can also be supplied to a PCM (Pulse Code Modulated) Tape Recorder for permanent record.

1-4. The MR312-Q1 can be interfaced to a computer through a control and data bus. The computer can then program the MR312-Q1 to output specific data at specific times, control a PCM Recorder, or control the outputs of a DA313-Q1 DAC in the remote MC314-Q1 Case.

1-5. Any channel's data word may be retrieved from the memory on a parallel output bus by means of a parallel input address code bus. New data overwrites old data so that the memory always has the most recent information.

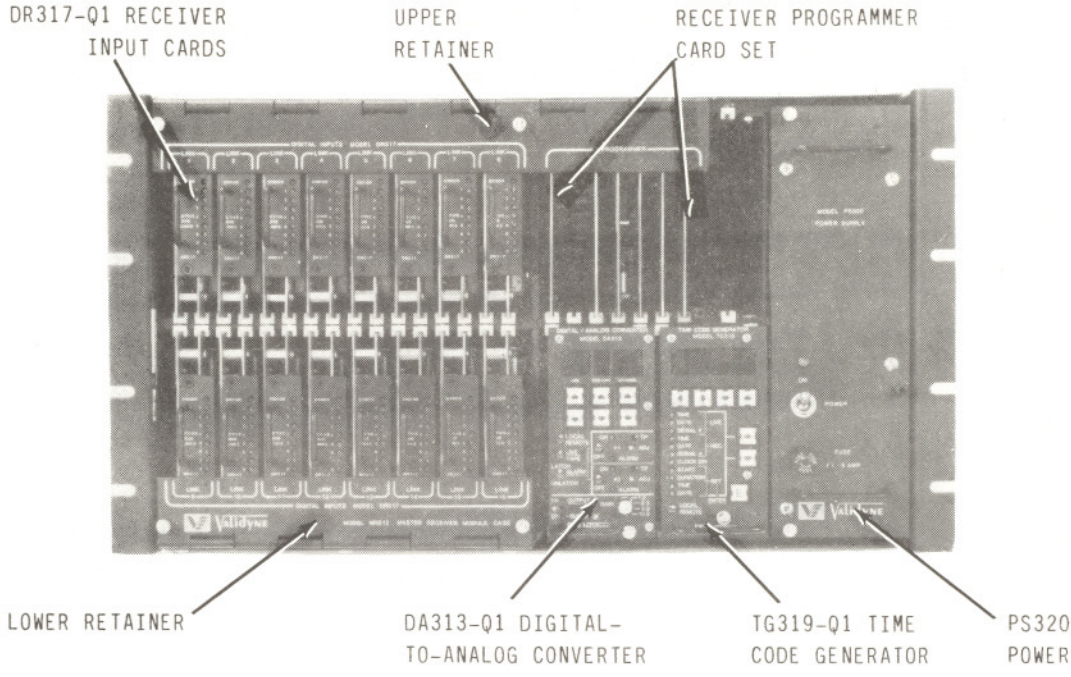
1-6. The MR312-Q1 can also store a program list of channel numbers to be addressed from memory. Up to 4096 channel address codes can be stored in a random manner as programmed by an external computer. An internal sequencer advances through a programmed memory, outputting a new channel address code each time the Programmer is strobed by the computer. This procedure allows selected channels from the MR312-Q1 to be fed into the computer's direct memory access port at a much higher rate than if under direct computer control.

1-7. GENERAL DESCRIPTION (SEE FIGURE 1-1).

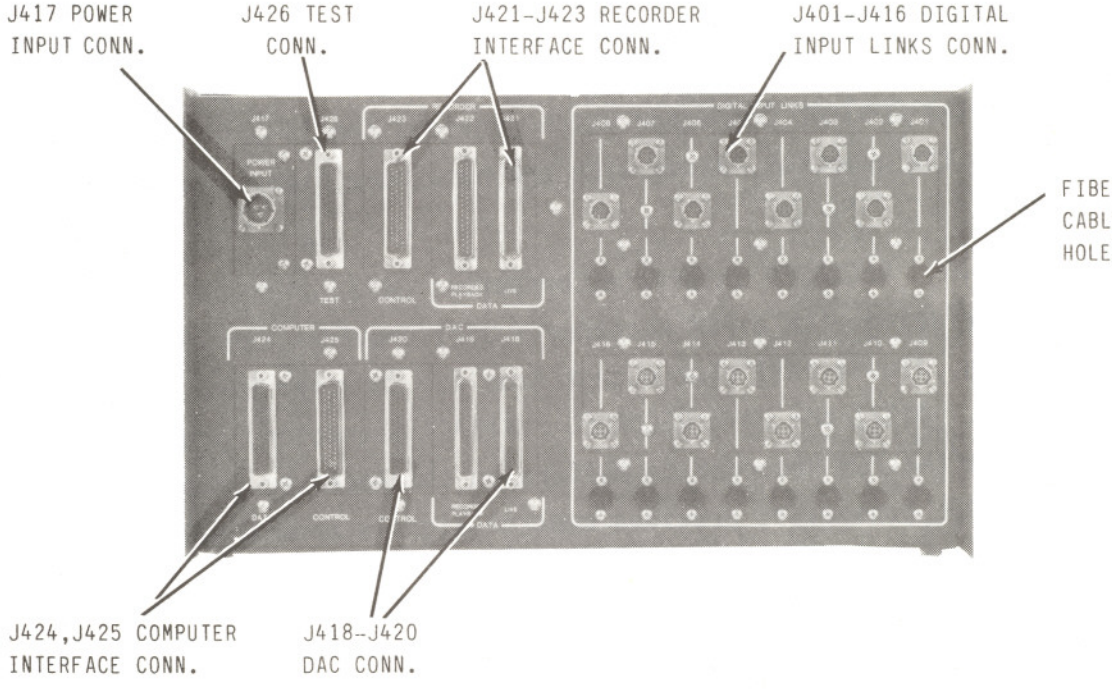
The MR312-Q1 is an all metal constructed case, designed for installation in a standard 19-inch equipment rack. The MR312-Q1 accepts up to 16 DR317-Q1 Receiver Cards (one for each input link), a Receiver Programmer Card set (see Paragraph 1-13 for description), an RC321 Tape Control Module, a DA313-Q1 Digital-to-Analog Converter Module, a TG319-Q1 Time Code Generator and a PS320-Q1 Power Supply Module.

1-8. Circuit boards and modules are inserted into card guides the front of the Master Receiver Case, and electrically connected to board edge connectors inside the case. The board edge connectors are so arranged that the various modules and circuit boards cannot accidently be inserted into the wrong connectors.

1-9. As shown in Figure 1-1, an upper retainer secures LINK 1-8 Receiver Input Cards, two Differential Driver Cards, Differential Receiver Card, Computer Interface Card, Control Sequencer Card and Address Generator Card. When an RC321 Tape Control Module is used in the system, the upper retainer is shorter in length, and the DR355-Q1 Differential Receiver Card and DD354 Differential Driver Card (located in slots J19 and J20) are shorter to accomodate the Tape Control Module. The



FRONT VIEW



REAR VIEW

Figure 1-1. MR312-Q1 Master Receiver, Front and Rear View.

lower retainer secures LINK 9-16 Receiver Input Cards. The Digital-to-Analog Converter Module, Time Code Generator Module, Tape Control Module, and Power Supply Module are held in place with captive screws installed on the modules.

1-10. All of the input and output connectors for the MR312-Q1 Master Receiver are located on the rear of the Master Receiver Case (see Figure 1-1). These consist of the following:

A. A POWER INPUT Connector J417 to provide 115 Vac to the Module Case.

B. DIGITAL INPUT LINKS Connectors J401 through J416 for digital data input into each Receiver Input Card. Each connector corresponds to an individual input card. J401 is LINK 1, J402 is LINK 2, etc. Access holes are also located underneath the connectors for inserting fiber optic cables if the Receiver Input Cards are equipped to receive fiber optic inputs.

C. Computer Interface Connectors J424 and J425. J424 is the DATA Connector which provides the 16 bit data word bus to the computer input port along with the handshake signals for the data bus. J425 is the CONTROL Connector which provides the 16-bit command word bus from the computer, along with the handshake signals for the command bus.

D. RECORDER Interface Connectors J421, J422 and J423 are for interfacing with a PCM Recorder. J421 provides the 16 links of live data, plus a real time output from the Receiver Cards to the PCM Recorder. J422, the DATA RECORDED PLAYBACK Connector, provides recorded data from the PCM Recorder to buffers on the Receiver Cards. J423, the CONTROL Connector, provides control signals from the Recorder Control Module to the PCM Recorder.

E. DAC Connectors J418, J419 and J420 are for interfacing with a remote MC314-Q1 DAC unit. J418, the LIVE DATA Connector, provides 16 links of live data to the DAC unit. J419, the RECORDED PLAYBACK DATA Connector, provides 16 links of recorded data to the DAC unit.

J420, the CONTROL Connector, provides the 16-bit command word bus to the DAC unit, and received through this connection are the DAC alarm and ready signals.

1-11. DR317-Q1 Receiver Input Cards (See Figure 3-1).

The Master Receiver accepts up to 16 separate DR317-Q1 Receiver Cards, one for each input link into the Receiver. Each Receiver Card can receive up to 256 data words (equivalent to eight Remote Multiplexers inputing into one MX311-Q1 Digital Submultiplexer) and store them in the random access memory (RAM) for controlled output to a computer. The number of Receiver Input Cards used in a particular system therefore depends upon the number of data input links being received by the Master Receiver.

1-12. The front of each Receiver Input Card has nine LED's labeled ERROR and ACTIVE SUB LINKS 1 through 8. The ERROR light illuminates when it detects an error in the link or sublink. This could be stoppage of transmission, or codes not being recognized properly such as when the ID portion does not match up with the input slot for a particular Receiver Input Card. Erroneous switch settings upstream of the Master Receiver or on the DR317-Q1 Receiver Input Card itself could also cause this. The eight ACTIVE SUB LINK lights (numbered 1 through 8) tell the operator which active sublinks are being received by the particular Receiver Card. In addition to the indicators, a toggle switch at the bottom of each Receiver Card is positioned for receiving data either from fiber optic cables or twisted-pair electrical cables. Eight miniature piano DIP switches mounted on the circuit board allow the operator to set the code for active sublinks that the Receiver Input Card will be receiving.

1-13. The Receiver Programmer Card Set consists of the following:

A. One DD354-Q1 Differential Driver Card (two DD354-Q1 Cards if a remote Digital-to-Analog Converter is used with the system). NOTE: a DD354-1-Q1 (long) Card is used if an RC321 Tape Control Module is NOT used, and a DD354-2-Q1 (short) Card is used if an RC321 Module IS used in the system.

B. One DR355-Q1 Differential Receiver Card. NOTE: a DR355-1-Q1 (long) Card is used if an RC321 Tape Control Module is NOT used, and a DR355-2-Q1 (short) Card is used if an RC321 Module IS used in the system.

C. One AG351-Q1 Address Generator Card.

D. One CI356-Q1 Computer Interface Card.

These cards essentially handle all of the interface bedtween the external computer and the HD310 System, and provide all synchronizing and control logic to allow a computer to retrieve data from the Master Receiver memory. The primary function of these cards is to interpret a direct request for specific data by the external computer, locate that data in the Master Receiver memory and output the data to the computer in a controlled manner.

1-14. DD354-Q1 Differential Driver and DR355-Q1 Differential Receiver Cards.

These two cards work together to provide a buffer function. The Differential Driver Card converts single-ended signals to differential signals for transmission outside the Master Receiver, while the Differential Receiver Card converts differential signals to single-ended signals for use by the Master Receiver. These cards combine to accept commands from the host computer, interpret and execute these commands, and provide the appropriate data. This is necessary when transmitting or receiving data over long transmission lines. An additional Differential Driver Card is used if the signal from the Master Receiver is transmitted to a remote Digital-to-Analog Converter. Additional information on these cards is contained in separate manuals.

1-15. AG351-Q1 Address Generator Card and CS348-Q1 Control Sequencer Cards.

The address Generator and Control Sequencer Cards are the heart of the Receiver Programmer, where information is stored and retrieved.

1-16. The Address Generator provides the addressing to the RAM on each Receiver Card to allow the transfer of the desired data to the host computer. This card works in conjunction with the Control Sequencer

Card. The Control Sequencer contains the microinstructions for each Type A and B command word. This card decodes the command word and performs the necessary control functions to the other modules of the Master Receiver. See Appendix A for Receiver Programmer/Remote Computer Interface format.

1-17. CI356-Q1 Computer Interface Card.

The Computer Interface Card is custom designed and may vary from system to system. It modifies the signal passing through the Receiver Programmer to make it compatible with the particular computer used with the system. It basically handles the different types of timing problems inherent with different computers. Appendix A gives the Receiver Programmer/Remote Computer Interface format. Additional information on the Computer Interface Card is contained in a separate manual which also lists the specification number of the card which is to be used with a particular computer.

1-18. RC321 Tape Control Module (Optional).

The RC321 Tape Control Module is located in the upper right hand side of the case assembly and provides remote control capabilities for the Honeywell 101 Computer used with the system. When used in the system, DD354-2-Q1 and DR355-2-Q1 short cards must be used (see Paragraph 1-13). Additional information on the module is contained in a separate manual.

1-19. DA313-Q1 Digital-to-Analog Converter (Optional).

Located in the lower right hand side of the case assembly is the DA313-Q1 Digital-to-Analog Converter. Its primary purpose, when used in the Master Receiver, is to convert differential data from any channel, link, or sublink to analog output data for testing and individual monitoring. additional information on the module is contained in a separate manual.

1-20. TG319-Q1 Time Code Generator. The Time Code Generator, located in the lower right hand corner of the Module Case, contains the interface for encoding real time clock data on the Pulse Code Modulated (PCM)

Recorder tape. By use of the Time Code Generator, the time (including seconds, minutes and hours), date (including day, month and year) and the Module Case serial number can be encoded with data to the PCM Recorder, and updated each millisecond. In the LIVE mode, this information is displayed on the front panel LED digital display, and permanently recorded on the tape for future reference.

1-21. When the tape is played back in the RECORD mode, the information encoded on the tape is displayed on the Time Code Generator LED digital display as an aid in locating the desired point on the tape. The Time Code Generator is also used to compensate for tape speed. This is accomplished by providing the different clock frequencies necessary to decode the various tape speeds.

1-22. Another function of the Time Code Generator is to set the time and duration "flag" or "interrupt" to the computer so that the MR312-Q1 Master Receiver and the computer communication can be started at the correct time. The timer information can be either real time from the Time Code Generator or recorded time from the tape.

1-23. The Time Code Generator also controls the distribution of data to the DA313-Q1 Digital-to-Analog Converter Module located within the MR312-Q1 Master Receiver. It also provides the 16 MHz master clock throughout the MR312 Module Case.

1-24. PS320-Q1 Power Supply Module.

The PS320-Q1 Power Supply Module occupies the entire right hand side of the module case and provides the ±15 Vdc and +5 Vdc operating power for the Master Receiver. Located on the front panel is the POWER ON Switch, which energizes the entire MR312-Q1 Master Receiver. The Power Supply Module slides into the module case and plugs into a board edge connector inside the case.

1-25. The PS320-Q1 contains two separate regulated DC power supplies which operate from 115 Vac. One supplies ±15 Vdc at ±0.3A and the other

supplies +5 Vdc at 40A. The DC outputs are isolated from each other and from the AC input, with the ±15 Vdc referred to an analog ground and the +5 Vdc referred to a separate digital ground.

1-26. Both of the DC power supplies in the PS320-Q1 are self-contained subassemblies which can be readily removed for repair or replacement. Additional information on the module is contained in a separate manual.

SECTION II
FUNCTIONAL DESCRIPTION

2-1. GENERAL.

Figure 2-1 is a functional block diagram of the MR312-Q1 Master Receiver showing the interaction between the various components within the receiver. Detailed in this section are functional descriptions of the DR317-Q1 Receiver Input Card and the Receiver Programmer Card Set (including the CS348-Q1 Control Sequencer Card and AG351-Q1 Address Generator Card). Functional Descriptions of the other components of the MR312-Q1 are described in separate manuals.

2-2. DR317-Q1 RECEIVER INPUT CARDS.

Up to 16 digital input signals from Remote Multiplexers or Submultiplexers enter the Master Receiver by direct electrical links or fiber optic cables. Each input is then directed to one of 16 DR317-Q1 Receiver Input Cards. There is one Receiver Input Card for each input link. The Receiver Input Card acquires the information, stores it in memory, and allows it to be accessed by means of the Receiver Programmer to the host computer.

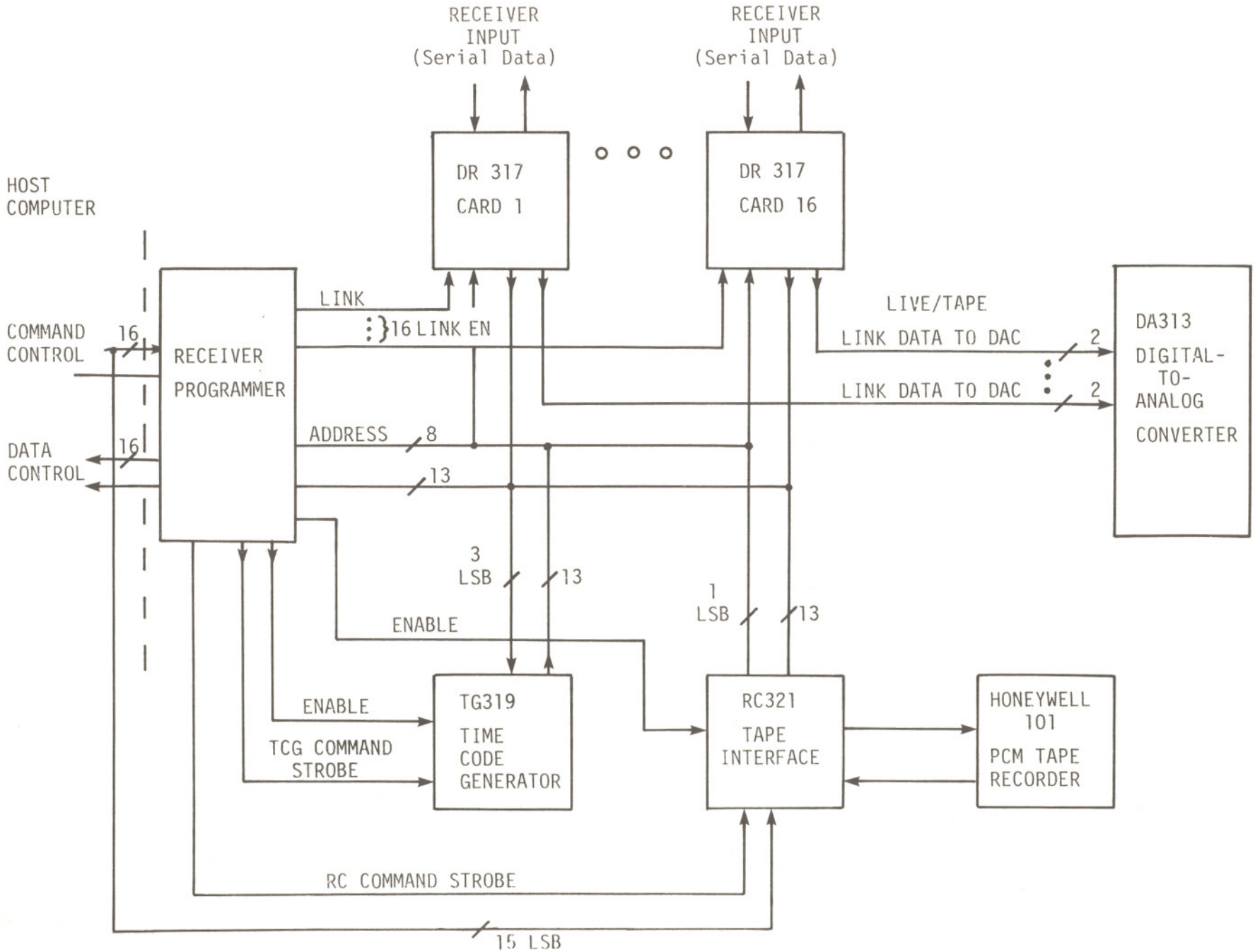
2-3. Each Receiver Card can receive and store up to 256 words (equivalent to eight Remote Multiplexers feeding a Digital Submultiplexer).

2-4. Each Receiver Card receives data in blocks representing one scan of all the active channels in a particular Remote Multiplexer unit. Each block of data (or scan) consists of a serial set of 14-bit words in the following order (see Figure 2-2).

A. One sync word indicating the start of a new scan.

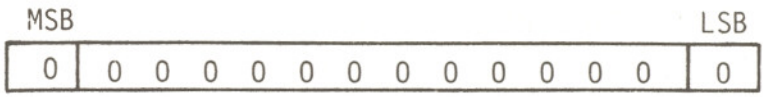
B. One identification word indicating the link designation, sublink designation, and number of active channels for the particular Remotte Multiplexer.

C. One data word for each active channel.

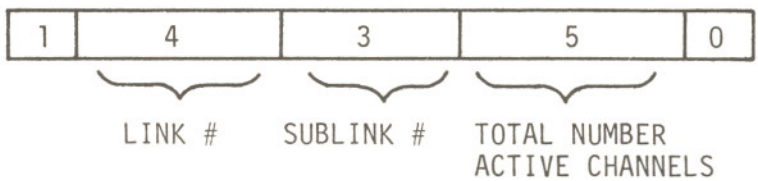

RECEIVER INPUT (Serial Data)
RECEIVER INPUT (Serial Data)
DR 317 CARD 1
DR 317 CARD 16
HOST COMPUTER
COMMAND CONTROL
16
RECEIVER PROGRAMMER
LINK
16 LINK EN
LIVE/TAPE
LINK DATA TO DAC
2
LINK DATA TO DAC
2
DA313 DIGITAL-TO-ANALOG CONVERTER
DATA CONTROL
16
ADDRESS
8
13
3 LSB
13
1 LSB
13
ENABLE
ENABLE
TCG COMMAND STROBE
TG319 TIME CODE GENERATOR
RC321 TAPE INTERFACE
HONEYWELL 101 PCM TAPE RECORDER
RC COMMAND STROBE
15 LSB

REMOTE MULTIPLEXER TO MASTER RECEIVER WORDS

Sync Word



ID Word



Data Word

DATA WORDS STORED IN MASTER RECEIVER RAM

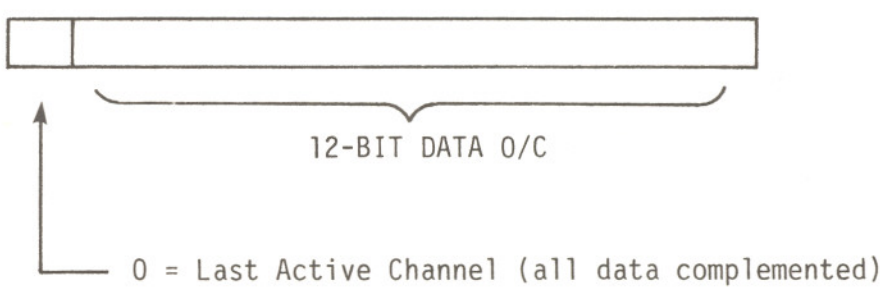


Figure 2-2. Receiver Card Word Formats.

2-5. Figure 2-3 is a functional block diagram of the Receiver Card and its interface. Live data enters the card by way of the RS422 input, or fiber optic input. The RS422/Fiber Optic Switch (S1) determines which type of signal the card will receive. The selected input is buffered and presented to the clock recovery and derandomizer circuitry.

2-6. The derandomized data then passes through a biphase generator from where the information can be presented to the Remote MC314-Q1 Digital-to-Analog Converter (DAC) Modules. An RS422 Buffer provides the randomized data to the tape recorder's input through connector J421 in the Master Receiver.

2-7. For the internal Digital-to-Analog Converter, a TTL output comes from each of the Receiver Cards to the DAC, for a total of 16 live or 16 PCM lines. An additional signal from the DA313 determines the selection of either live or PCM on all 16 of the Receiver Cards simultaneously.

2-8. Following derandomization, output is fed into a data selector which selects the recovery clock, and the live or PCM data (playback from tape). The data selector decides whether data is live or PCM from the PR PCM line from the Receiver Programmer. The host computer can decide whether it wants to receive live or PCM data.

2-9. Data then goes into the serial-to-parallel shift registers. The serial data stream consists of a synchronizing (sync) word (all zeros) followed by an identification word containing the link and sublink numbers and the maximum (last) channel number, followed by the channel data word. Word length is 14 bits as follows:

Sync Word = 14 zeros
ID Word = Leading "1"
Link number (4 bits)
Sublink number (3 bits)
Last channel number (5 bits)
Following "0"
Data = Leading "1", 12 data bits and following "zero"

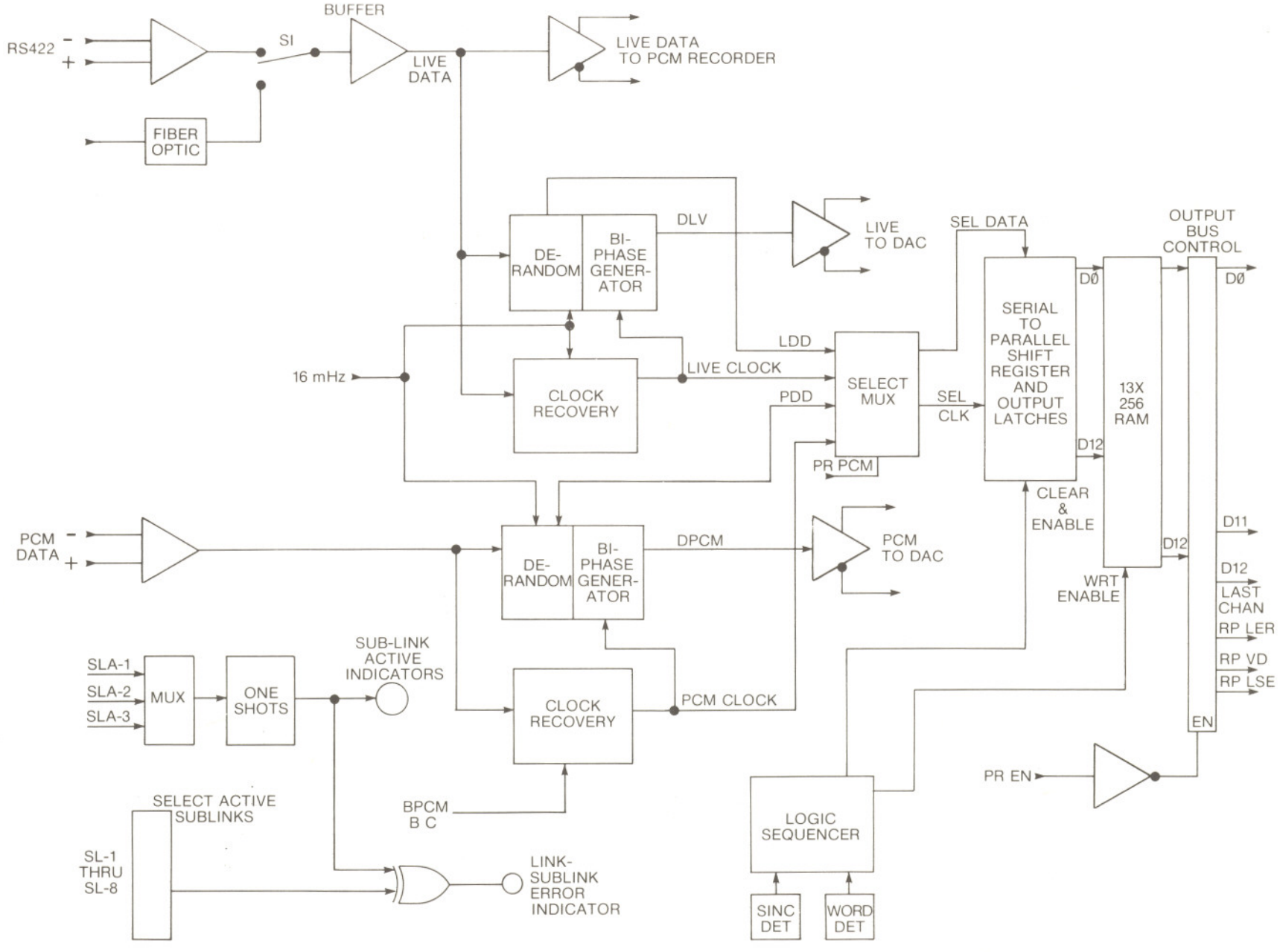


Figure 2-3. DR317-Q1 Receiver Input Cards, Functional Block Diagram.

2-10. A logic sequencer is utilized for all logical decision functions such as what to do when a sync word or data word is detected. Table 2-1 and Figure 2-4 show the flow sequence of the DR317-Q1 Logic Sequencer.

2-11. Information is then taken out of the shift register and loaded into a holding register (output latches). During the same logic sequence, the information is taken out of the shift register and loaded into the memory.

2-12. The "Open Collector Inverters to Data Buss" is common to all Receiver Cards. It allows the selected Receiver Card to transmit its data, as determined by the PR EN line, from the Receiver Programmer.

2-13. The Active Sublink information derived from the ID word provides the input to a decoder whose output triggers one shots. This in turn drives the sublink active LED's. Each time a sublink comes in, the one shot is triggered and the LED is turned on. The sublink information is provided to the addressing during the loading of the data into the RAM. The sublink one shots also provide an input to a two input exclusive OR gate acting as a comparator. The other input comes from a piano switch which is set to indicate whether or not the sublink is active. If any one of the sublinks being received does not match its particular switch setting, the red error LED turns on. Each slot has a link number hard-wired to the card edge connector, and this feeds a comparator on the card, comparing it to incoming link ID. The red error LED also turns on when the link being received does not match the dedicated link slot into which the card is plugged.

2-14. RECEIVER PROGRAMMER CARD SET (SEE FIGURE 2-5).

2-15. Computer Interface - Computer Commands.

The primary function of the Receiver Programmer is to interpret a direct request for specific data by a computer, locate that data in the Master Receiver and output the data to the computer in a controlled manner.

Table 2-1. DR317-Q1 Logic Sequencer.

LOGIC STATE	
0	Wait for word detect.
01	Issue synchronized word detect.
01	Load Max Channel into holding (U11A) Reg.
01	Load Sublink ID into holding (U28A) Reg.
01	Load Link ID into holding (U20) Reg. for Link Error Check.
01	Update (Trigger) Link Active (U-3A) One Shot (Sublink Enable Detect).
1	Increment Channel Counter (U26A).
1	Reset Input Shift Registers (U10A, U18A).
2	Wait for Sync detect or word detect.
20	Sync detect - go to State 0.
20	Enable current active Sublink (U1-B) on display.
24	Word detect - go to State 4.
4	State 4 go to State 1.
4	Enable write/read disable circuit.
4	Load Channel and Sublink into address reg. (U29A) thus presenting address for data in memory at end of State 4.
4	Load data in memory registers (U13, U21) thus presenting data to memory at end of State 4.

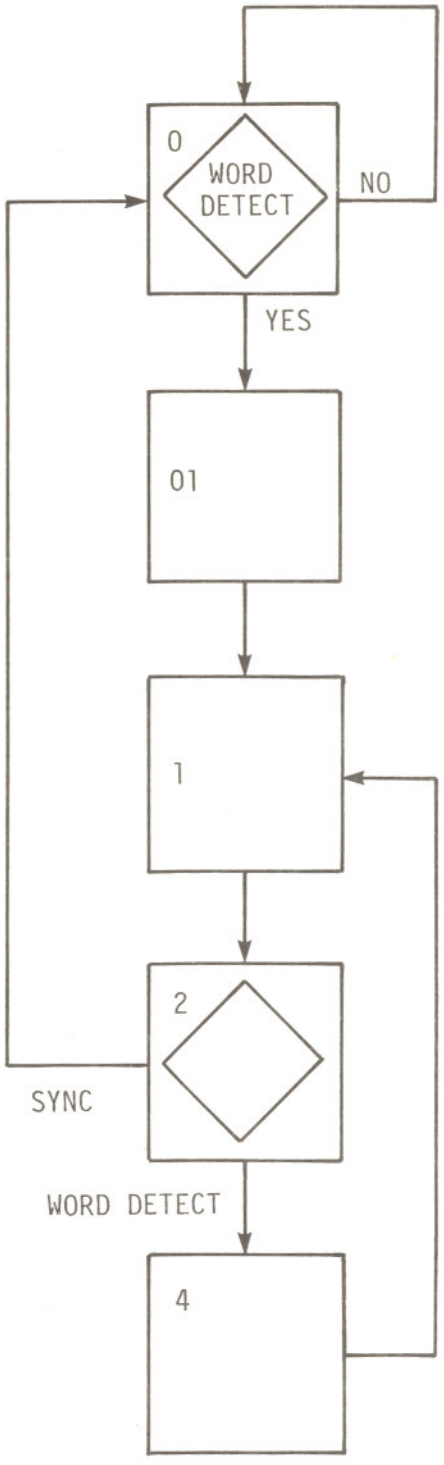


Figure 2-4. DR317-Q1 Receiver Input Card, Sequencer Flow Diagram.

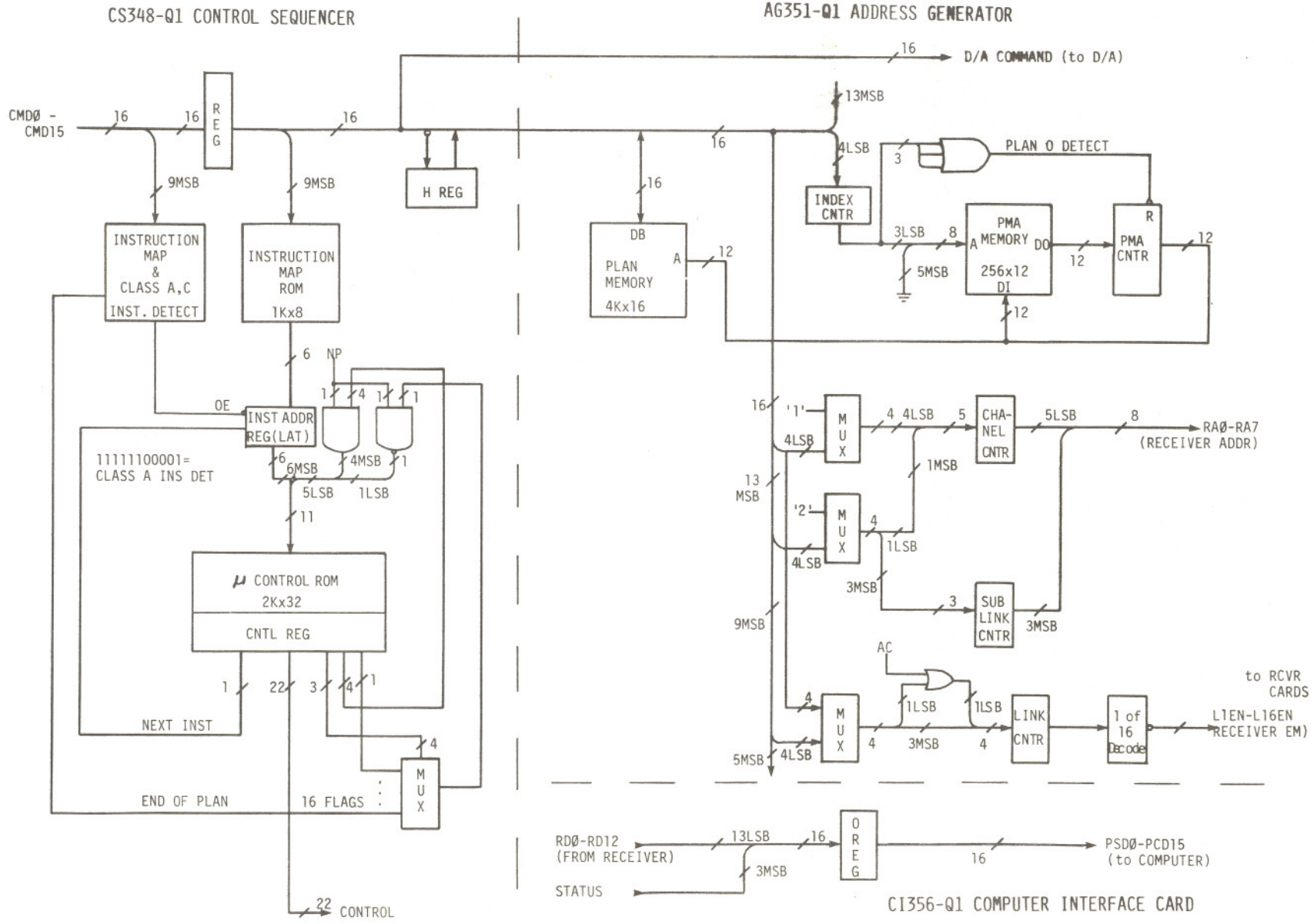


Figure 2-5. Receiver Programmer, Functional Block Diagram.

2-16. There are several methods by which a computer may request a specific channel or groups of channels to be output from the Master Receiver. Each method is initiated by the computer through the use of Group A commands. Any time the Receiver Programmer receives a Group A control word it will terminate any ongoing output and execute the specific request for data as explained below. (See Appendix A for word formats.)

2-17. Direct Data Request. The Receiver Programmer will respond to a two-word command which will initiate transmission of specific data to the computer. The first word is a Group A control word which will indicate that a Direct Data Request is to be made. The second is a Group B word which tells the Receiver Programmer what data is required, and can be any one of the data requests listed below:

A. Single Channel Request

The Receiver Programmer will output data corresponding to a single data channel. The format for the allowed data request words is given in Appendix A.

B. Time Request

The Receiver Programmer will output one of four different time words, corresponding to either the current time or tape recorded time, allowing for time correlation of data being monitored.

C. Link Data Request

By using a Link Request word, the computer may request data for all active channels on a given link. The Receiver Programmer will output one data word for each active channel starting with Channel 1 of Sublink 1 for the given link. The first data word transmitted will be coded for "start-of-scan", "start-of-link" and "start-of-sublink". When it has output data for all active channels in Sublink 1, it will output a data word for Channel 1 of Sublink 2, coding this word as "start-of-sublink", and then output one word for each active channel of Sublink 2. This will continue until it has gone through all active channels of the given link. Any time it encounters a sublink with no active channels, it will output a data word with a "start of sublink" and the error bit set to indicate "error", and then go to the next sublink.

In this way the computer will receive at least one word for each sublink and will be able to tell how many channels are active for each sublink in any given link.

2-18. All Channel Requests. This request is identified by a single Group A control word (see Appendix A), and will cause the Receiver Programmer to output all active channels for all 16 links. The data is output in the same manner as in the Link Request Case, with the "start-of-link" code explained previously. In this mode, at least one word for each sublink of each link will be generated with each inactive sublink marked by the error bit.

2-19. Sample Plan Requests. The Receiver Programmer is capable of storing up to 4096 specific data requests for information in up to 16 different groups or sample plans to be accessed by a single control word from the computer. Each step of a sample plan can be:

A. Single Channel Request

B. Link Request

C. PCM Footage

2-20. The computer first loads these sets of instructions into the Receiver Programmer memory by using a "Load Plan" command, followed by the random set of Group B data request words which will make up that particular sample plan, and an end of plan word as the last entry of each sample plan. The sample plan can be changed at any time provided that all sample plans are reloaded each time.

2-21. After the plans are stored in the Receiver Programmer memory, the computer can initiate execution of any sample plan by simply outputting a "READ PLAN" command identifying the desired sample plan. The Receiver Programmer will then execute each data request listed in the Sample Plan just like it was a direct request by the computer. This allows for monitoring of specific pre-selected channels within a minimum of computer-generated requests and thus maximizes data through-put rate.

2-22. Digital-to-Analog Control. The computer can select the data channel that any individual Digital-to-Analog Converter in the MC314-Q1 Module Case is to monitor. The computer accomplishes this by transmitting a two-word command. The first word identifies which DAC module case and module it wants to change and the second word tells that DAC module which link, sublink and data channel it should monitor. These commands are known as Group C commands and are detailed in Appendix A.

2-23. Computer Interface - Data Transmission.

After the Receiver Programmer has interpreted the computer's request for data, it will output one data word for each channel or time information requested via a 16-bit parallel data buss into the computer's Direct Memory Access (DMA) or parallel I/O port. Each 16-bit word transmitted will contain 12 bits of data and 4 error/status bits (see Appendix A). The word transmission rate can be synchronized through the use of an external transfer clock which is generated by the computer.

2-24. A control line from the computer to the Receiver Programmer will indicate whether each request for data should be executed once (i.e., single scan) or continuously. This control line should be set to "continuous" for reliable interface. If continuously, the Receiver Programmer will re-execute the last computer request for data continuously until a new Group A command is received.

2-25. The output of data to the computer can also be controlled from the computer through the use of Start and Duration time words (see Paragraph 1-22).

2-26. Computer Interface Control and Status Lines.

Table 2-2 gives a brief description of the function of each control and status line used in interfacing the Master Receiver (by means of the Receiver Programmer) to a computer. All control lines may be set to be either active-high or active-low depending on the requirements of the particular computer. Figure 2-6 shows the interaction.

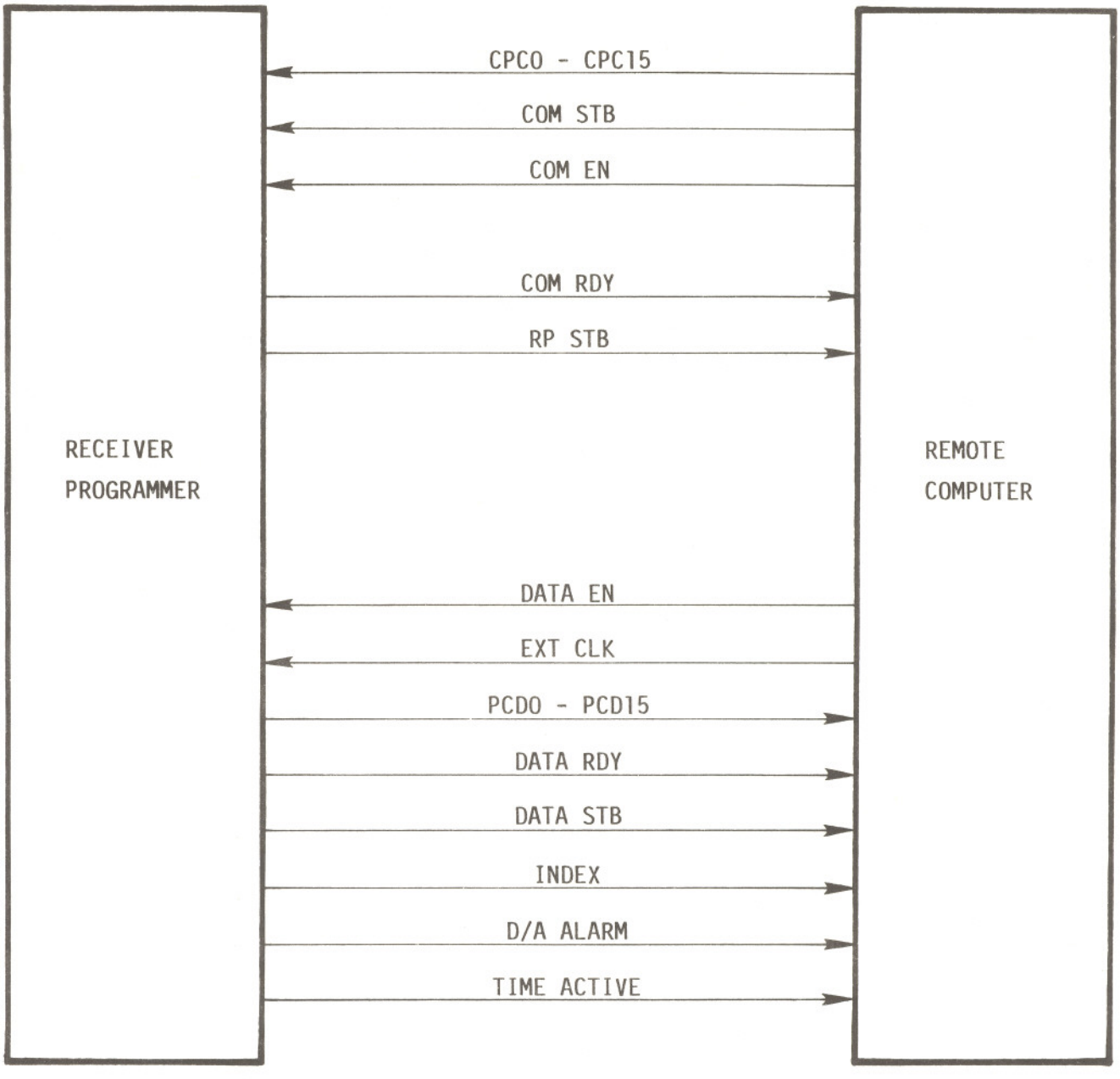


Figure 2-6. Receiver Programmer to Remote Computer Interface.

Table 2-2. Control and Status Lines.

COM EN:	This signal is generated by the computer and enables Receiver Programmer to receive a command.
COM RDY:	The Receiver Programmer generates this signal to inform the computer that it is ready to receive command.
COM STB:	Computer issues this strobe to the Receiver Programmer to initiate the internal command receiving clock. The Receiver Programmer clocks a command into its command register at the low to high transition of the COM STB. A command word has to be maintained valid for a minimum of 220 ns after the COM STB goes high.
RP STROBE:	A clock from the Receiver Programmer used in generating a Command Strobe by the remote computer. It can also be used as the Command Strobe into the Receiver Programmer directly, and as a data received link to the remote computer.
EXT CLK:	The clock provided by the remote computer to receive data.
DATA EN:	This signal is generated by the computer to enable the Receiver Programmer to start data output.
DATA RDY:	The Receiver Programmer replies to the computer by activating the DATA RDY after it receives an active DATA EN. At this time, the programmer is ready to transmit sample data to the computer.
DATA STB:	Data is strobed to the computer when the DATA STB is low. Data is stable for 1 usec. The DATA STB position and pulse width are adjustable.
INDEX:	This is a synchronizing pulse. A low pulse is generated when the receiver is processing Sublink 1 of the selected link. The link is selected by the command issued by the computer. The pulse width is 125 ns.

Table 2-2. Control and Status Lines (Continued).

D/A ALARM:	When the D/A input level passes through a predetermined threshold, D/A ALARM is activated, providing the alarm function is enabled.
TIME ACTIVE:	When the real time in the Time Code Generator equals the start time, the signal will be high and stay high until the duration time is expired. NOTE: Pins 40 and 41 are for internal use only.

2-27. Computer Interface - Data Transmission Timing.

A. Command Cycle Timing.

The remote computer issues a command to the Receiver Programmer by activating the COM EN. The Receiver Programmer replies by activating the COM RDY, indicating that it is ready to receive a command. During command transmission, COM STD is used as a clock to strobe command words to the Receiver Programmer. The minimum hold time for the command after COM STD is returned to a high state is 220 ns.

B. Data Cycle Timing.

The computer initiates the data transfer by activating the DATA EN. The Receiver Programmer responds by activating the DATA RDY to indicate that it is ready to transmit data. The transmission is synchronized to the clock supplied by the remote computer. The remote computer can terminate the data cycle by deactivating the DATA EN. If DATA EN is deactivated before the DATA RDY is deactivated, the data transmission is suspended. If a new Type A command is issued before DATA EN is active, the suspended output cycle will be terminated.

2-28. Interface Capabilities. The interface signals between the Master Receiver and the host computer are conformed to the RS422A interface standard. The differential drivers and receivers are capable of transmitting data at 1 MHz rate for a distance of up to 400 feet using standard RS422A qualified cable. The drivers are capable of driving 110 ohms

of termination. However, each receiver is terminated by a 180 ohm resistor.

2-29. An interface unit is available to convert differential signals to single-ended TTL signals. The driver output components are 50 ohm drivers and the receivers have one LSTTL equivalent input loads with a 1 k ohm pull up resistor to +5 Vdc. This unit is intended to be used when the host computer is only configured for single-ended TTL signals.

2-30. AG351-Q1 Address Generator Card (See Figure 2-7).

The AG351-Q1 Card supplies the addressing to the Receiver Cards and also stores the program plans. When a Start Plan command is transmitted to the Master Receiver, it enters on the Control Word Bus, and inputs to this Card by way of the Control Sequencer. The plan number is decoded and the starting address of this plan is found. With the Start Address loaded into the Address Register, the RAM storing the plan itself can be accessed and the plan can be run. Each RAM can store up to sixteen plans of instruction. The Control Sequencer is used to load the RAM and perform the instructions stored there.

2-31. When a single channel is requested, the address is selected by a Mux and then fed to the Receiver Card on the address bus, which holds the information. The sequencing of this procedure is handled by the Control Sequencer. The link that the data is received on is determined, and the link enable output turns on that particular Receiver Card. This process is performed for all data retrievals, whether by direct or planned commands.

2-32. CS348-Q1 Control Sequencer Card (See Figure 2-8).

The CS348-Q1 Card accepts the control word bus from the computer after it has been buffered by the Differential Receiver Card. The common words are on this bus (see Appendix A). Depending upon the type of command sent, this card will respond by initiating and sequencing various control signals to complete the function desired. Control signals are provided for the Time Code Generator Module, Remote Tape Control Module,

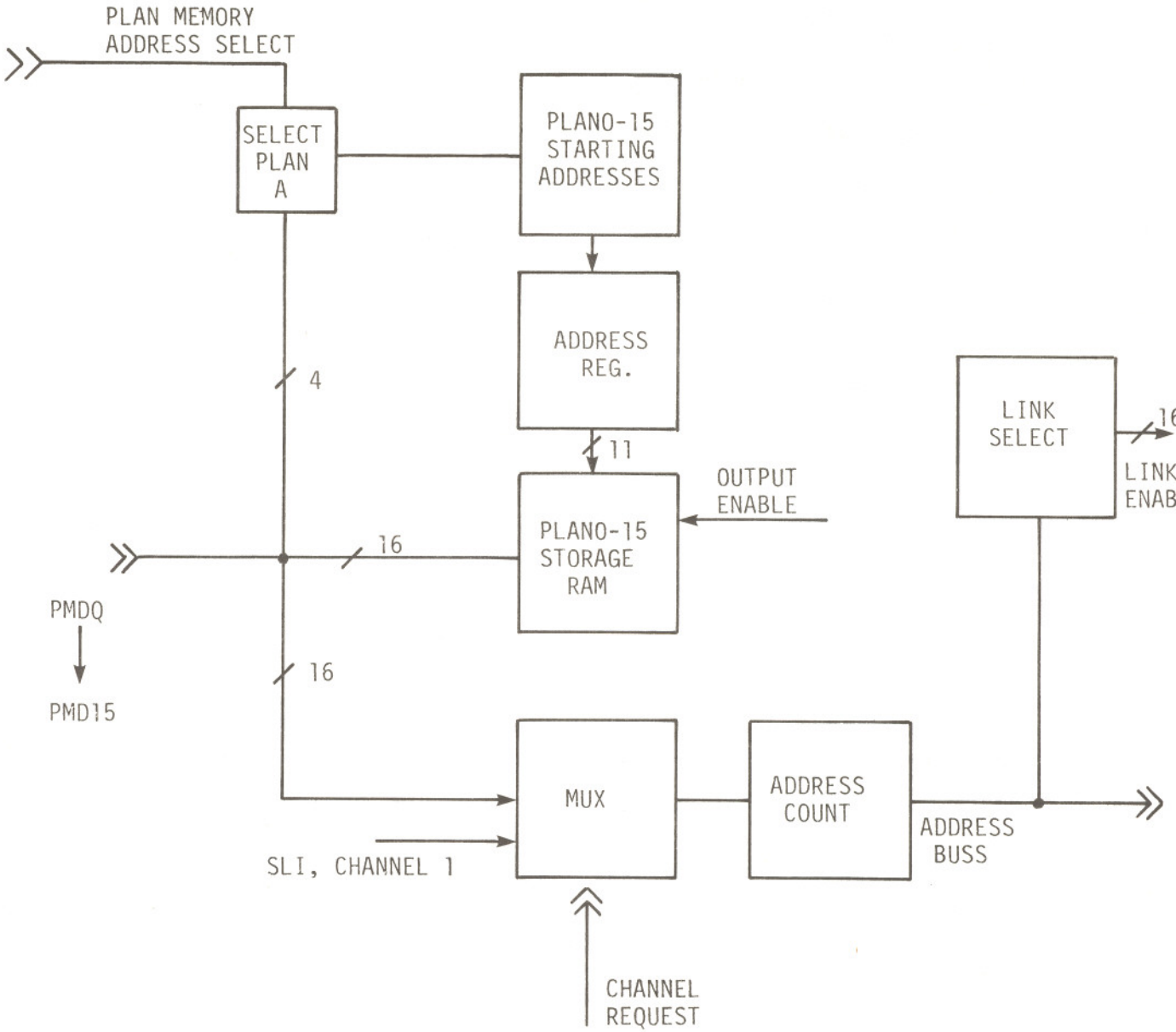


Figure 2-7. AG351-Q1 Address Generator Card, Functional Block Diagram.

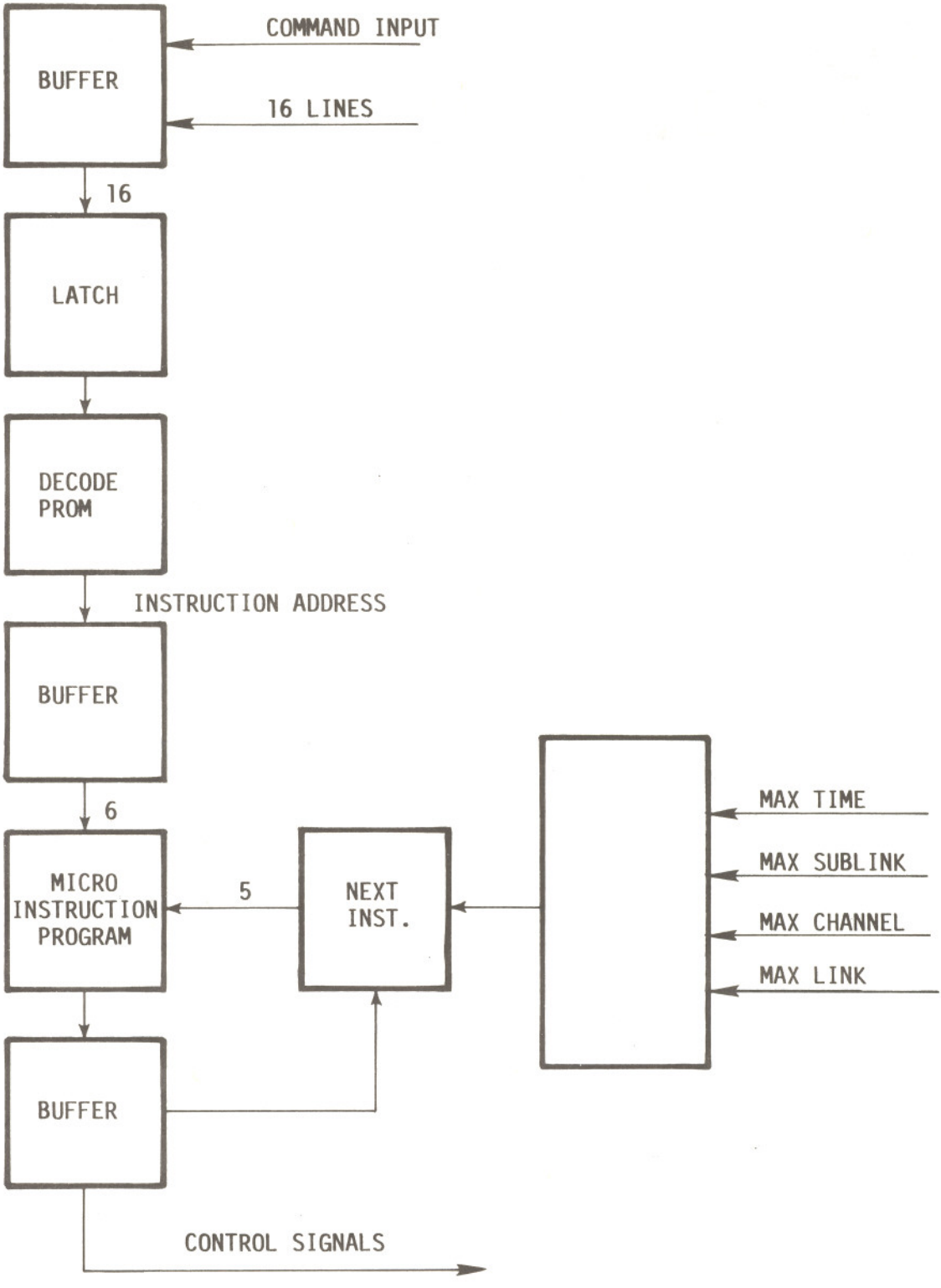


Figure 2-8. CS348-Q1 Control Sequencer Card, Functional Block Diagram.

and Address Generator. The Control Sequencer also accepts inputs from the Address Generator where appropriate.

2-33. CI356-Q1 Computer Interface Card.

The Computer Interface Card is a customized card designed to interface various computers. Each card is designed to interface a specific computer as required. More complete information is contained in a separate manual.

3-1. INSPECTION AND MOUNTING.

On receipt of MR312-Q1 Master Receiver and optional modules, remove the unit and its modules from their packing and inspect for any damage in shipment.

3-2. The equipment has been thoroughly inspected and tested before leaving the factory. Any damage should be reported to your carrier immediately. Visually check for any broken connectors. Remove any foreign matter, such as packing material, from the Master Receiver and its modules.

3-3. The MR312-Q1 can be either rack-mounted or used as is on a bench. For rack mounting, all that is required for installation is to remove the four rubber feet on the module case (if installed), and secure the Master Receiver to a standard 19-inch relay rack with eight screws at the front (and eight screws at the rear if seismic protection is desired).

3-4. INSTALLING CIRCUIT BOARDS AND MODULES.

If circuit boards and modules have not been installed in the MR312-Q1 Master Receiver, installation should be accomplished in the following order:

CAUTION

ALWAYS REMOVE POWER FROM MR312-Q1 BEFORE REMOVAL OR INSTALLATION OF ANY CIRCUIT BOARD, PLUG-IN MODULE OR FIBER OPTIC CABLE. THIS IS ACCOMPLISHED BY SWITCHING POWER SWITCH ON PS320-Q1 POWER SUPPLY TO THE OFF POSITION.

3-5. PS320-Q1 Power Supply Installation.

A. Slide the PS320-Q1 Power Supply into the opening on the right hand side of the module case. The Power Supply rides on an upper

and lower guide at the left side of slot position. Make sure the left side circuit board lines up properly with its guides before sliding into case.

B. Slide the Power Supply all the way to the rear of the case until the circuit board engages with the board edge connector inside the case. Secure the PS320-Q1 Power Supply into the module case by tightening the two captive bolt fasteners at the front panel.

3-6. Receiver Programmer Card Set and RC321 Tape Control Module Installation.

The Receiver Programmer section consists of a series of circuit boards which must be inserted in the upper section of the module case in the PROGRAMMER area. Before insertion, lift the upper retainer on the module cased to gain access to the card guides. Upper retainer is held in place by two captive screws. When installing board or modules, slide boards all the way back until they make electrical contact with the board edge connectors inside the module case. All boards or modules are keyed so that they cannot be inserted into the wrong connector.

A. Insert the DD354-2-Q1 Differential Driver Card (short card) into slot J20 in the module case. Use the DD3545-1-Q1 (long card) when RC321 Tape Control Module is not used with the system.

B. Insert the DR355-2-Q1 Differential Receiver Card (short card) into slot ~~J109~~ J19. Use the DR355-1-Q1 (long card) when RC321 Tape Control Module is not used with the system.

C. Insert the RC321 Tape Control Module (if used with the system) into slots J19 and J20.

D. Insert the AG351-Q1 Address Generator Card into slot J18.

E. Insert the CS348-Q1 Control Sequencer Card into slot J17. Slot J31 should be empty.

F. Insert CI356-Q1 Computer Interface Card into slot J32.

G. Insert DD354-Q1 Differential Driver Card (long card) into slot J30.

3-7. TG319-Q1 Time Code Generator Installation.

Insert TG319-Q1 Time Code Generator module into slots J23 and J26. Slide the module all the way back until the circuit boards fully engage the board edge connectors inside the case.

3-8. DA313-Q1 Digital-to-Analog Converter Module (Optional) Installation.

If a DA313-Q1 Digital-to-Analog Converter Module is used in the MR312-Q1, slide the module into slot J22 and the guide located to the right of J22. Slide the module all the way back until the circuit board fully engages the board edge connector inside the case. Tighten captive screw.

NOTE

To aid in installation, apply pressure to left side of module when sliding it into Master Receiver Module Case.

3-9. If a DA313-Q1 Digital-to-Analog Converter Module is not used with the system, J22 slot will remain empty.

3-10. DR317-Q1 Receiver Cards Installation (See Figure 3-1).

Before installing DR317-Q1 Receiver Cards, set the following switches on the circuit board.

A. If input to the Master Receiver and DR317-Q1 Receiver Cards is via fiber optic cable, set the OPTICAL/DIFF Switch on the DR317-Q1 Board to OPTICAL. If input is via electrical cable (differential), set the switch to DIFF.

B. Set the eight DIP Switches on the DR317-Q1 Board to correspond to the number of active sublinks which will be connected to the particular Receiver Card. Example: If the signal to be fed to the particular Receiver Card is originating from a Digital Submultiplexer with active sublinks 1 through 4, the DIP Switch numbers 1, 2, 3 and 4 on the Receiver Card must be set to the active position. If signal is originating from a Digital Submultiplexer with active sublinks 1 through

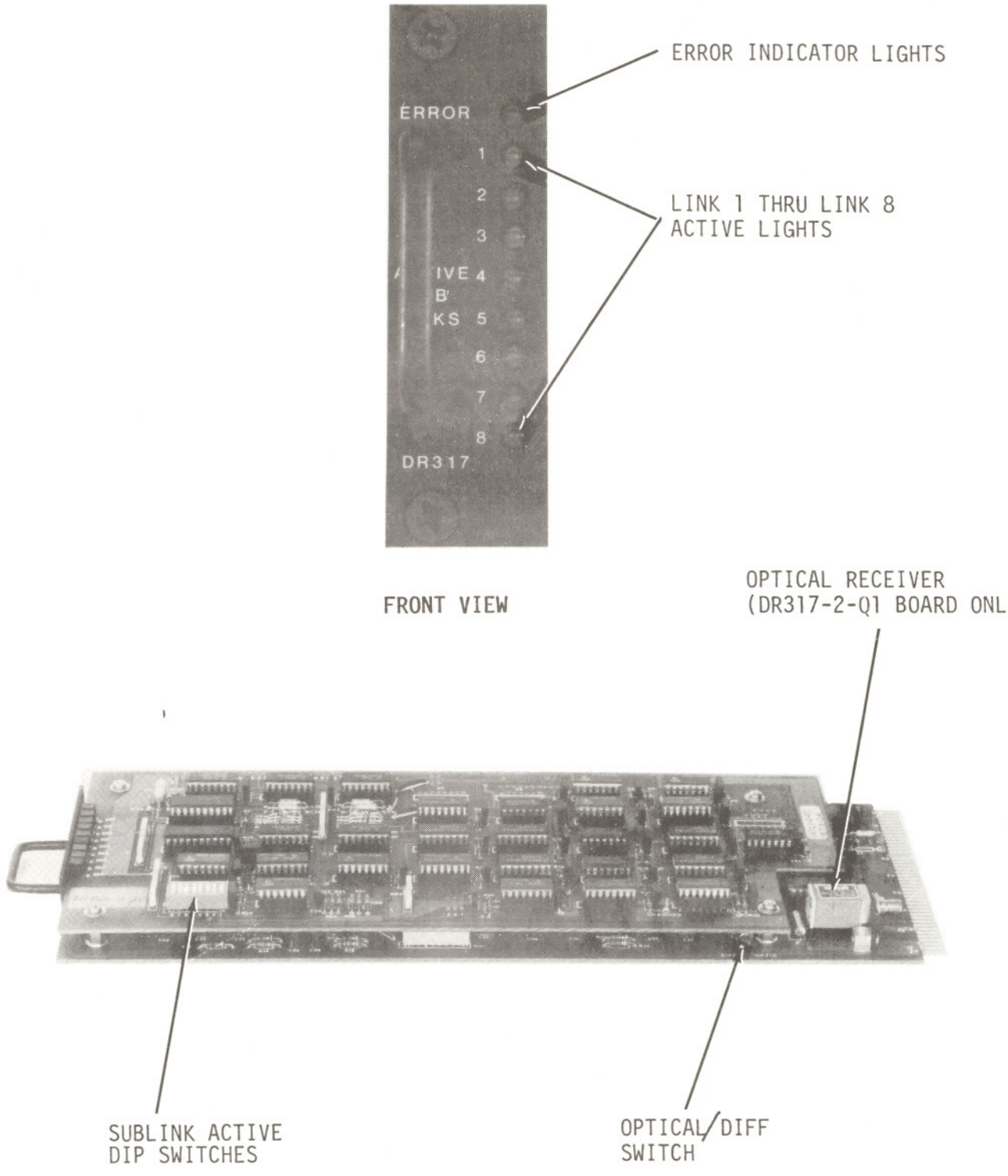


Figure 3-1. DR317-Q1 Receiver Card, Installation.

8, the DIP Switch numbers 1, 2, 3, 4, 5, 6, 7 and 8 must be set to the active position, etc. The position of the DIP Switches must always correspond to the number of the active sublinks originating from the Multiplexer. If the signal is coming directly from the Remote Multiplexer without first going through a Submultiplexer, only sublink 1 on the DIP Switch must be placed in the active position.

C. To set the DIP Switches, move the particular switch (numbered 1 through 8 corresponding to the LINK number) to the OPEN position if the sublink is active and toward the NUMBER position if the sublink is inactive.

3-11. Installation of DR317-Q1 Receiver Cards without Fiber Optic Connections.

If the signal to the DR317-Q1 Receiver Card is coming from an electrical input and not from a fiber optic input, the Receiver Card can be directly plugged into one of the LINK slots where data input is desired (Link 1 through Link 16). When inserting Receiver Cards, make sure that each card is fully seated in the mating board edge connector inside the case.

3-12. Installation of DR317-Q1 Receiver Cards with Fiber Optic Connections.

If the signal to the DR317-Q1 Receiver Card is coming from a fiber optic cable, install board as follows:

A. Make sure the DR317-Q1 Receiver is marked -2 and has an optical receiver installed, or card will not accept optical input.

B. At the rear of the module case, feed the fiber optic cable from the Multiplexer or Submultiplexer through the access hole directly below the electrical input connector for the particular Receiver Card. Example: To install a fiber optic cable to LINK 1, fiber optic cable must pass through opening beneath connector J401.

CAUTION

ALWAYS REMOVE POWER FROM THE MR312-Q1 (TURN SWITCH OFF IN THE PS320-Q1 POWER SUPPLY) BEFORE CONNECTING OR DISCONNECTING ANY PLUG-IN MODULE OR BEFORE INSERTING OR REMOVING FIBER OPTIC CABLES.

NOTE

The last two digits of the DIGITAL INPUT LINKS Connector number correspond to the LINK number on the front of the module case where the DR317-Q1 Receiver Cards are installed. Example: Connector J402 goes to LINK No. 2, J413 to LINK No. 13, etc.

C. Cable should be inserted until it projects through the front of the module case.

D. Locate the optical receiver on the DR317-2 Receiver Card. Inspect the connector interface on the optical receiver and the open end of the fiber optic cable to verify absence of foreign matter.

E. Install fiber optic cable onto the receiver receptacle and tighten bushing nut. Verify OPTIC/DIFF Switch is set to OPTIC.

F. Install DR317-2 Receiver Card into module case, making sure the circuit board is firmly installed in board edge connector inside module case. Feed excess optical cable out the rear of the module case while inserting card.

CAUTION

FIBER OPTIC CABLE CAN BE BROKEN IF BENT TOO SHARPLY. TAKE CARE IN HANDLING.

G. The above steps should be repeated for each Receiver Card for which fiber optic reception is desired.

3-13. When all DR317 Receiver Cards have been installed, along with the Receiver Programmer Cards and RC321 Tape Control Module (if used),

re-install the upper and lower retainers over the Receiver Cards, and secure in position with captive screws. The MR312-Q1 Master Receiver is now ready for electrical hookup.

3-14. INPUT/OUTPUT CONNECTIONS.

3-15. J417 Power Input Connection.

The Master Receiver is furnished with a three-pin Bendix PT02A-12-3P (or equivalent) Power Input Connector. Fabricate a three-wire power cable to the furnished PT06-type mating connector, and electrically wire the opposite end into a 115 Vac, 60 Hz power source, as shown for J417 in Figure 3-2. Plug the cable into the J417 POWER INPUT receptacle.

CAUTION

BE SURE THE THIRD (GREEN) WIRE IS TIED INTO APPROPRIATE CHASSIS GROUND FOR SAFETY.

3-16. DIGITAL INPUT LINKS, Electrical Connections.

Connectors J401 through J416 accept the digital input data for each DR317-Q1 Receiver Input Card. The last two digits of the input connector number correspond with the link number slot to which the Receiver Input Card is installed. Example: Connector J401 provides an input to Receiver Card installed in LINK No. 1; Connector J410 provides an input to Receiver Card installed in LINK No. 10, etc.

3-17. Sixteen 4-pin PT02-type bulkhead connectors are furnished with the Master Receiver for wiring in the data input. Wire each connector used according to Figure 3-2 Connectors J401 through J416.

3-18. In the basic HD310 System, where Digital Submultiplexers are not used, connect J401 to Remote Multiplexer No. 1, J402 to Remote Multiplexer No. 2, etc. Make sure a Receiver Card is installed for each data input.

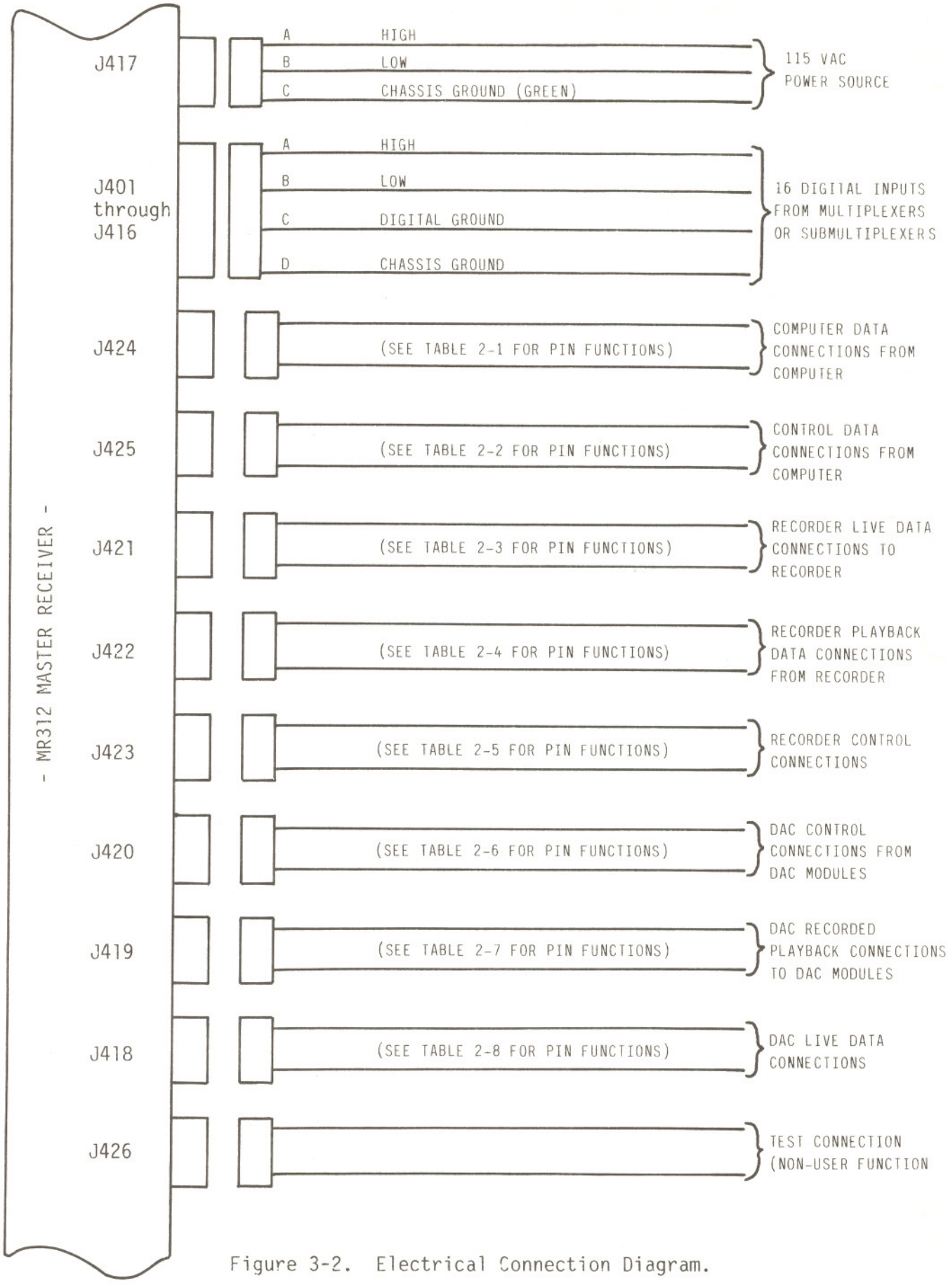


Figure 3-2. Electrical Connection Diagram.

3-19. In the expanded HD310 System, where Digital Submultiplexers are used, connect J401 to Digital Submultiplexer No. 1, J402 to Digital Submultiplexer No. 2, etc. Each Digital Submultiplexer should have from 2 to 8 Remote Multiplexers connected to it.

3-20. If digital input connections are made through fiber optic cables, see Paragraph 3-12.

3-21. COMPUTER Interface Connections.

Each MR312 Master Receiver contains two 50-pin type "D" subminiature rectangular connectors for interface with a processor or computer. J424 provides all I/O lines necessary to enable the Receiver Programmer section of the Master Receiver to transmit data to the computer or processor, and J425 provides all I/O lines necessary to enable the Receiver Programmer section to receive commands from the computer or processor.

3-22. If the computer used with the system cannot accept differential signals a DB344 Differential-to-Single Ended Converter must be connected between the computer and Connectors J424 and J425 (see Figure 3-3) to convert the signal to single-ended. If DB344 is installed, PCM/DIGITAL Switch on the DB344 must be in the DIGITAL position.

3-23. J424 COMPUTER DATA Connections. There are 16 pairs of lines for transmission of the 160-bit data words, and five pairs of lines for control and status between the Receiver Programmer and the computer. Three pairs of lines are available for custom interfaces as well as two pins tied to signal ground. Table 3-1 gives the pin assignments.

3-24. Connect up to 50 wires to a mating connector and connect to the computer as described in the table.

3-25. J425 CONTROL DATA Connections. There are 16 pairs of lines for receiving the 16-bit command or control words, and five pairs of lines for control and status between the Receiver Programmer and the computer. There are also three pairs of lines for custom interfacing as well as two pins tied to signal ground. Table 3-2 gives the pin assignments.

Table 3-1. J424 Connector Data/Computer.
(50 PIN - FEMALE)

Pin #	Signal Name	Hi/Lo	Function	Activated By
1	PCD0	L	Data Word - Bit 0 (LSB)	Receiver Programmer
2	PCD0	H	Data Word - Bit 0	Receiver Programmer
3	PCD1	L	Data Word - Bit 1	Receiver Programmer
4	PCD1	H	Data Word - Bit 1	Receiver Programmer
5	PCK2	L	Data Word - Bit 2	Receiver Programmer
6	PCK2	H	Data Word - Bit 2	Receiver Programmer
7	PCD3	L	Data Word - Bit 3	Receiver Programmer
8	PCD3	H	Data Word - Bit 3	Receiver Programmer
9	PCD4	L	Data Word - Bit 4	Receiver Programmer
10	PCD4	H	Data Word - Bit 4	Receiver Programmer
11	PCD5	L	Data Word - Bit 5	Receiver Programmer
12	PCD5	H	Data Word - Bit 5	Receiver Programmer
13	PCD6	L	Data Word - Bit 6	Receiver Programmer
14	PCD6	H	Data Word - Bit 6	Receiver Programmer
15	PCD7	L	Data Word - Bit 7	Receiver Programmer
16	PCD7	H	Data Word - Bit 7	Receiver Programmer
17	GND		Signal Ground	
18	PCD8	H	Data Word - Bit 8	Receiver Programmer
19	PCD8	L	Data Word - Bit 8	Receiver Programmer
20	PCD9	H	Data Word - Bit 9	Receiver Programmer
21	PCD9	L	Data Word - Bit 9	Receiver Programmer
22	PCD10	H	Data Word - Bit 10	Receiver Programmer
23	PCD10	L	Data Word - Bit 10	Receiver Programmer
24	PCD11	H	Data Word - Bit 11	Receiver Programmer
25	PCD11	L	Data Word - Bit 11	Receiver Programmer
26	PCD12	L	Data Word - Bit 12	Receiver Programmer
27	PCD12	L	Data Word - Bit 12	Receiver Programmer
28	PCD13	H	Data Word - Bit 13	Receiver Programmer
29	PCD13	L	Data Word - Bit 13	Receiver Programmer
30	PCD14	H	Data Word - Bit 14	Receiver Programmer
31	PCD14	L	Data Word - Bit 14	Receiver Programmer
32	PCD15	H	Data Word - Bit 15	Receiver Programmer
33	PCD15	L	Data Word - Bit 15 (MSB)	Receiver Programmer
34	$\overline{\text{Data En}}$	H	Data Enable	Computer
35	$\overline{\text{Data En}}$	L	Data Enable	Computer
36	$\overline{\text{Data Rdy}}$	H	Data Ready	Receiver Programmer
37	$\overline{\text{Data Rdy}}$	L	Data Ready	Receiver Programmer
38	$\overline{\text{Data Stb}}$	H	Data Strobe	Receiver Programmer
39	$\overline{\text{Data Stb}}$	L	Data Strobe	Receiver Programmer
40				
41				
42	D/A Alarm	H	DAC Alarm Flag	Receiver Programmer
43	D/A Alarm	L	DAC Alarm Flag	Receiver Programmer
44				
45				
46			Not Assigned	
47			Not Assigned	
48			Not Assigned	
49			Not Assigned	
50	GND		Signal Ground	

Table 3-2. J425 Connector Control Computer
(50 PIN - Male)

Pin #	Signal Name	Hi/Lo	Function	Activated By
1	CPC0	L	Command Word - Bit 0 (LSB)	Computer
2	CPC0	H	Command Word - Bit 0	Computer
3	CPC1	L	Command Word - Bit 1	Computer
4	CPC1	H	Command Word - Bit 1	Computer
5	CPC2	L	Command Word - Bit 2	Computer
6	CPC2	H	Command Word - Bit 2	Computer
7	CPC3	L	Command Word - Bit 3	Computer
8	CPC3	H	Command Word - Bit 3	Computer
9	CPC4	L	Command Word - Bit 4	Computer
10	CPC4	H	Command Word - Bit 4	Computer
11	CPC5	L	Command Word - Bit 5	Computer
12	CPC5	H	Command Word - Bit 5	Computer
13	CPC6	L	Command Word - Bit 6	Computer
14	CPC6	H	Command Word - Bit 6	Computer
15	CPC7	L	Command Word - Bit 7	Computer
16	CPC7	H	Command Word - Bit 7	Computer
17	GND		Signal Ground	
18	CPC8	H	Command Word - Bit 8	Computer
19	CPC8	L	Command Word - Bit 8	Computer
20	CPC9	H	Command Word - Bit 9	Computer
21	CPC9	L	Command Word - Bit 9	Computer
22	CPC10	H	Command Word - Bit 10	Computer
23	CPC10	L	Command Word - Bit 10	Computer
24	CPC11	H	Command Word - Bit 11	Computer
25	CPC11	L	Command Word - Bit 11	Computer
26	CPC12	H	Command Word - Bit 12	Computer
27	CPC12	L	Command Word - Bit 12	Computer
28	CPC13	H	Command Word - Bit 13	Computer
29	CPC13	L	Command Word - Bi5 13	Computer
30	CPC14	H	Command Word - Bit 14	Computer
31	CPC14	L	Command Word - Bit 14	Computer
32	CPC15	H	Command Word - Bit 15	Computer
33	CPC15	L	Command Word - Bit 15 (MSB)	Computer
34	$\overline{\text{Com. Stb}}$	H	Command Strobe	Computer
35	$\overline{\text{Com. Stb}}$	L	Command Strobe	Computer
36	$\overline{\text{Com. En}}$	H	Command Enable	Computer
37	$\overline{\text{Com. En}}$	L	Command Enable	Computer
38	$\overline{\text{Ext. Clk}}$	H	External Clock	Computer
39	$\overline{\text{Ext. Clk}}$	L	External Clock	Computer
40		H		Internal Use Only
41		L		Internal Use Only
42	$\overline{\text{Com. Rdy}}$	H	Command Ready	Recv'r Programmer
43	$\overline{\text{Com. Rdy}}$	L	Command Ready	Recv'r Programmer
44	$\overline{\text{RP STB}}$	H	Receiver Strobe	Recv'r Programmer
45	$\overline{\text{RP STB}}$	L	Receiver Strobe	Recv'r Programmer
46			Not Assigned	
47			Not Assigned	
48			Not Assigned	
49			Not Assigned	
50	GND		Signal Ground	

3-26. Connect up to 50 wires to mating connector and connect to the computer as described in the table.

3-27. RECORDER Interface Connections.

Each MR312 Master Receiver contains three type "D" subminiature rectangular connectors for interfacing with a PCM Recorder. Two connectors (J421 and J422) transmit data to and from the recorder, and one connector (J423) provides the control functions to operate the recorder.

3-28. If the recorder used with the system cannot accept differential signals, a DB344 Differential-to-Single Ended Converter must be connected between the recorder and Connectors J421 and J422 (see Figure 3-3) to convert the signal to single-ended. If DB344 is installed, PCM/DIGITAL Switch on the DB344 must be in the PCM position.

3-29. J421 RECORDER LIVE DATA Connections. The J421 Connector is a 37-pin Type D female connector which provides 16 pairs of lines for transmission of serial data to the recorder, one for each input data link into the Master Receiver. Another pair of lines transmits serial time data in parallel to the 16 data channels, and one pin is tied to signal ground. Two pins are not used. Table 3-3 gives the pin assignments.

3-30. Connect up to 37 wires to a mating connector, and connect to the input of the PCM Recorder or DB344 Differential-to-Single Ended Converter as described in the table.

3-31. J422 RECORDER PLAYBACK DATA Connections. The J422 Connector is a 37-pin Type D female connector which provides the same functions as the JX-3 for transmission of recorded data back to the Master Receiver during the playback mode. Table 3-4 gives the pin assignments.

3-32. Connect up to 37 wires to a mating connector and connect to the output of the PCM Recorder or DB344 Differential-to-Single Ended Converter.

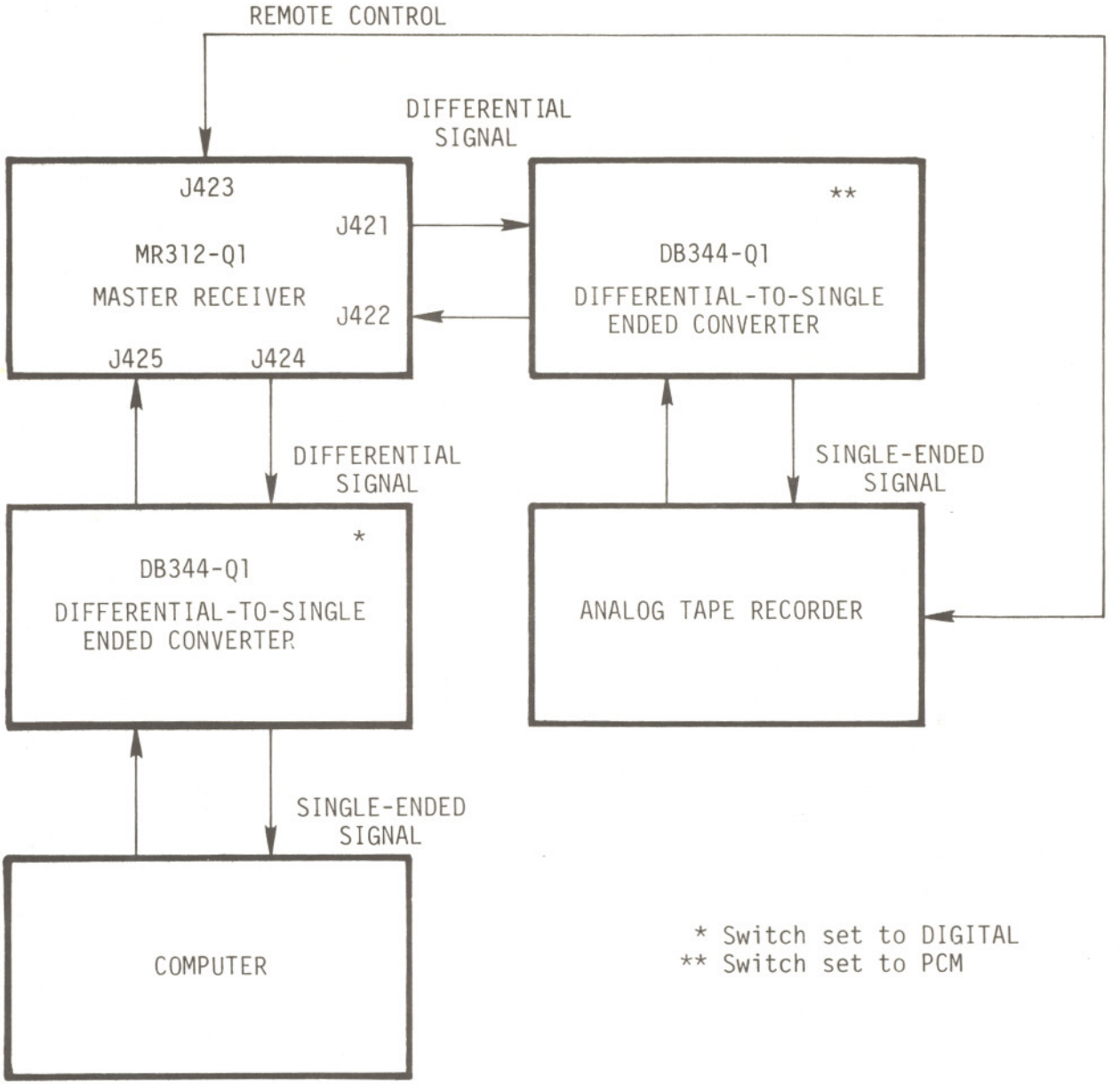


Figure 3-3. Connection Diagram for DB344 Differential-to-Single Ended Converter.

Table 3-3. J421 Connector Live Data/Recorder.

(37 PIN - FEMALE)				
Pin #	Signal Name	Hi/Lo	Function	Activated By
1	MRREC1	L	Link 1 Live Data	Rec. Card #1
2	MRREC1	H	Link 1 Live Data	Rec. Card #1
3	MRREC2	L	Link 2 Live Data	Rec. Card #2
4	MRREC2	H	Link 2 Live Data	Rec. Card #2
5	MRREC3	L	Link 3 Live Data	Rec. Card #3
6	MRREC3	H	Link 3 Live Data	Rec. Card #3
7	MRREC4	L	Link 4 Live Data	Rec. Card #4
8	MRREC4	H	Link 4 Live Data	Rec. Card #4
9	MRREC5	L	Link 5 Live Data	Rec. Card #5
10	MRREC5	H	Link 5 Live Data	Rec. Card #5
11	MRREC6	L	Link 6 Live Data	Rec. Card #6
12	MRREC6	H	Link 5 Live Data	Rec. Card #6
13	MRREC7	L	Link 7 Live Data	Rec. Card #7
14	MRREC7	H	Link 7 Live Data	Rec. Card #7
15	MRREC8	L	Link 8 Live Data	Rec. Card #8
16	MRREC8	H	Link 8 Live Data	Rec. Card #8
17	MRREC9	L	Link 9 Live Data	Rec. Card #9
18	MRREC9	H	Link 9 Live Data	Rec. Card #9
19	GND		Signal Ground	
20	MRREC10	H	Link 10 Live Data	Rec. Card #10
21	MRREC10	L	Link 10 Live Data	Rec. Card #10
22	MRREC11	H	Link 11 Live Data	Rec. Card #11
23	MRREC11	L	Link 11 Live Data	Rec. Card #11
24	MRREC12	H	Link 12 Live Data	Rec. Card #12
25	MRREC12	L	Link 12 Live Data	Rec. Card #12
26	MRREC13	H	Link 13 Live Data	Rec. Card #13
27	MRREC13	L	Link 13 Live Data	Rec. Card #13
28	MRREC14	H	Link 14 Live Data	Rec. Card #14
29	MRREC14	L	Link 14 Live Data	Rec. Card #14
30	MRREC15	H	Link 15 Live Data	Rec. Card #15
31	MRREC15	L	Link 15 Live Data	Rec. Card #15
32	MRREC16	H	Link 15 Live Data	Rec. Card #16
33	MRREC16	L	Link 16 Live Data	Rec. Card #16
34	Time	H	Real Time	Time Code Gen.
35	Time	L	Real Time	Time Code Gen.
36			Not Assigned	
37			Not Assigned	

Table 3-4. J422 Connector Playback Data Recorder.

(37 PIN - MALE)				
Pin #	Signal Name	Hi/Lo	Function	Activated By
1	RECMR1	L	Link 1 Recorded Data	Recorder
2	RECMR1	H	Link 1 Recorded Data	Recorder
3	RECMR2	L	Link 2 Recorded Data	Recorder
4	RECMR2	H	Link 2 Recorded Data	Recorder
5	RECMR3	L	Link 3 Recorded Data	Recorder
6	RECMR3	H	Link 3 Recorded Data	Recorder
7	RECMR4	L	Link 4 Recorded Data	Recorder
8	RECMR4	H	Link 4 Recorded Data	Recorder
9	RECMR5	L	Link 5 Recorded Data	Recorder
10	RECMR5	H	Link 5 Recorded Data	Recorder
11	RECMR6	L	Link 6 Recorded Data	Recorder
12	RECMR6	H	Link 6 Recorded Data	Recorder
13	RECMR7	L	Link 7 Recorded Data	Recorder
14	RECMR7	H	Link 7 Recorded Data	Recorder
15	RECMR8	L	Link 8 Recorded Data	Recorder
16	RECMR8	H	Link 8 Recorded Data	Recorder
17	RECMR9	L	Link 9 Recorded Data	Recorder
18	RECMR9	H	Link 9 Recorded Data	Recorder
19	GND		Signal Ground	
20	RECMR10	H	Link 10 Recorded Data	Recorder
21	RECMR10	L	Link 10 Recorded Data	Recorder
22	RECMR11	H	Link 11 Recorded Data	Recorder
23	RECMR11	L	Link 11 Recorded Data	Recorder
24	RECMR12	H	Link 12 Recorded Data	Recorder
25	RECMR12	L	Link 12 Recorded Data	Recorder
26	RECMR13	H	Link 13 Recorded Data	Recorder
27	RECMR13	L	Link 13 Recorded Data	Recorder
28	RECMR14	H	Link 14 Recorded Data	Recorder
29	RECMR14	L	Link 14 Recorded Data	Recorder
30	RECMR15	H	Link 15 Recorded Data	Recorder
31	RECMR15	L	Link 15 Recorded Data	Recorder
32	RECMR16	H	Link 16 Recorded Data	Recorder
33	RECMR16	L	Link 16 Recorded Data	Recorder
34	RECTME	H	Recorded Time Data	Recorder
35	RECTME	L	Recorded Time Data	Recorder
36			Not Assigned	
37			Not Assigned	

3-33. J423 RECORDER CONTROL Connections. The J423 Connector is a 50-pin male connector which provides the tape control and status functions to enable a computer or processor to control the recorder via the Receiver Programmer in the Master Receiver. Table 3-5 gives the pin assignments.

3-34. Connect up to 50 wires to a mating connector and connect to the control line of the PCM Recorder.

3-35. MC314-Q1 Digital-to-Analog Converter (DAC) Module Interface Connections.

Each MR312-Q1 Module Case contains three type "D" subminiature rectangular connectors J418, J419 and J420 for interfacing with the MC314-Q1 DAC Module Cases. These connectors transmit "live" or "recorded" playback data to the DA313-Q1 Digital-to-Analog Converters as well as providing for control of the DAC's by the computer or processor.

3-36. J420 DAC CONTROL Connections. J420 is a 50-pin type "D" female connector which provides the interface between the computer and the DAC modules via the RP315-Q1 Receiver Programmer. It contains 16 pairs of lines for transmission of control words to the DAC's, four pairs of lines for control and DAC status functions, and two pins tied to signal ground. Table 3-6 gives the pin assignments.

3-37. Connect up to 50 wires to a mating connector and connect to the MC314-Q1 DAC Module Case. If more than one MC314-Q1 DAC Module Case is used with the system, they can be serially connected together as shown in Figure 3-4.

3-38. J419 DAC RECORDED PLAYBACK DATA Connections. The J419 is a 37-pin type "D" female connector which provides serial data output to the DAC Modules from the Master Receiver. In the case of the JD-2 Connector, the data is "playback" data coming from the recorder over 16 pairs of parallel lines, one pair for each data link input into the Master Receiver. Table 3-7 gives the pin assignments.

Table 3-5. J423 Connector Control/Recorder.

(50 PIN - MALE)				
Pin #	Signal Name	Hi/Lo	Function	Activated By
1	GND			
2	REC IND		Record Indicator	Tape Drive
3	GND			
4	FWD IND		Forward Indicator	Tape Drive
5	GND			
6	FOOTAGE RST		Footage Reset	Remote Control
7	GND			
8	REV ACT		Reverse Activate	Remote Control
9	GND			
10	U2 CONT		Turn 2nd MSD On	Tape Drive
11	GND			
12	U1 & U5 CONT		Turn Sign, MSB & 5th (LSD) Digit On	Tape Drive
13	GND			
14	D1		Bit One of Digit	Tape Drive
15	GND			
16	SIGN		Sign Bit of Digit	Tape Drive
17	GND			
18	REV IND		Reverse Indicator	Tape Drive
19	GND			
20	REMOTE CON-L		To Indicate that Remote Control is Enable	Remote Control
21	GND			
22	FAST ACT		Fast Switch Activate	Remote Control
23	GND			
24	STOP ACT		Stop Switch Active	Remote Control
25	GND			
26	U4 CONT		Turn On 4th Digit	Tape Drive
27	GND			
28	D2		Bit Two of Digit	Tape Drive
29	GND			
30	U6 BLANKING		Turn Off Sign & MSD	Tape Drive
31	GND			
32	NC		Not Assigned	
33	GND			
34	FAST IND		Fast Indicator	Tape Drive
35	GND			
36	STOP IND		Stop Indicator	Tape Drive
37	GND			
38	RECORD ACT		Record Activate	Remote Control
39	GND			
40	FORWARD ACT		Forward Activate	Remote Control
41	GND			
42	U3 CONT		Turn On 3rd Digit	Tape Drive
43	GND			
44	D3		Bit 3 of Digit	Tape Drive
45	GND			
46	D0		Bit 1 (LSB) of Digit	Tape Drive
47	GND			
48	U7 BLANKING		Turn Off U5 (LSD)	Tape Drive
49	GND			
50	GND			

Table 3-6. J420 Connector Control/DAC.

(50 PIN - FEMALE)				
Pin #	Signal Name	Hi/Lo	Function	Activated By
1	PDD0	L	DAC Command Word - Bit 0 (LSB)	Recv'r Prgmr
2	PDD0	H	DAC Command Word - Bit 0	Recv'r Prgmr
3	PDD1	L	DAC Command Word - Bit 1	Recv'r Prgmr
4	PDD2	H	DAC Command Word - Bit 1	Recv'r Prgmr
5	PDD2	L	DAC Command Word - Bit 2	Recv'r Prgmr
6	PDD2	H	DAC Command Word - Bit 2	Recv'r Prgmr
7	PDD3	L	DAC Command Word - Bit 3	Recv'r Prgmr
8	PDD3	H	DAC Command Word - Bit 3	Recv'r Prgmr
9	PDD4	L	DAC Command Word - Bit 4	Recv'r Prgmr
10	PDD4	H	DAC Command Word - Bit 4	Recv'r Prgmr
11	PDD5	L	DAC Command Word - Bit 5	Recv'r Prgmr
12	PDD5	H	DAC Command Word - Bit 5	Recv'r Prgmr
13	PDD6	L	DAC Command Word - Bit 6	Recv'r Prgmr
14	PDD6	H	DAC Command Word - Bit 6	Recv'r Prgmr
15	PDD7	L	DAC Command Word - Bit 7	Recv'r Prgmr
16	PDD7	H	DAC Command Word - Bit 7	Recv'r Prgmr
17	GND		Signal Ground	
18	PDD8	H	DAC Command Word - Bit 8	Recv'r Prgmr
19	PDD8	L	DAC Command Word - Bit 8	Recv'r Prgmr
20	PDD9	H	DAC Command Word - Bit 9	Recv'r Prgmr
21	PDD9	L	DAC Command Word - Bit 9	Recv'r Prgmr
22	PDD10	H	DAC Command Word - Bit 10	Recv'r Prgmr
23	PDD10	L	DAC Command Word - Bit 10	Recv'r Prgmr
24	PDD11	H	DAC Command Word - Bit 11	Recv'r Prgmr
25	PDD11	L	DAC Command Word - Bit 11	Recv'r Prgmr
26	PDD12	H	DAC Command Word - Bit 12	Recv'r Prgmr
27	PDD12	L	DAC Command Word - Bit 12	Recv'r Prgmr
28	PDD13	H	DAC Command Word - Bit 13	Recv'r Prgmr
29	PDD13	L	DAC Command Word - Bit 13	Recv'r Prgmr
30	PDD14	H	DAC Command Word - Bit 14	Recv'r Prgmr
31	PDD14	L	DAC Command Word - Bit 14	Recv'r Prgmr
32	PDD15	H	DAC Command Word - Bit 15	Recv'r Prgmr
33	PDD15	L	DAC Command Word - Bit 15 (MSB)	Recv'r Prgmr
34	PDDS	H	Command Strobe	MC314 Case
35	PDDS	L	Command Strobe	
36	DPRDY	H	DAC Ready	MC314 Case
37	DPRDY		DAC Ready	
38	ALARM 1*	H	DAC Alarm 1	MC314 Case
39	ALARM 1*		DAC Alarm 1	
40	ALARM 2*	H	DAC Alarm 2	Recv'r Prgmr
41	ALARM 2*	L	DAC Alarm 2	Recv'r Prgmr
42			Not Assigned	
43			Not Assigned	
44			Not Assigned	
45			Not Assigned	
46			Not Assigned	
47			Not Assigned	
48			Not Assigned	
49			Not Assigned	
50	GND		Signal Ground	

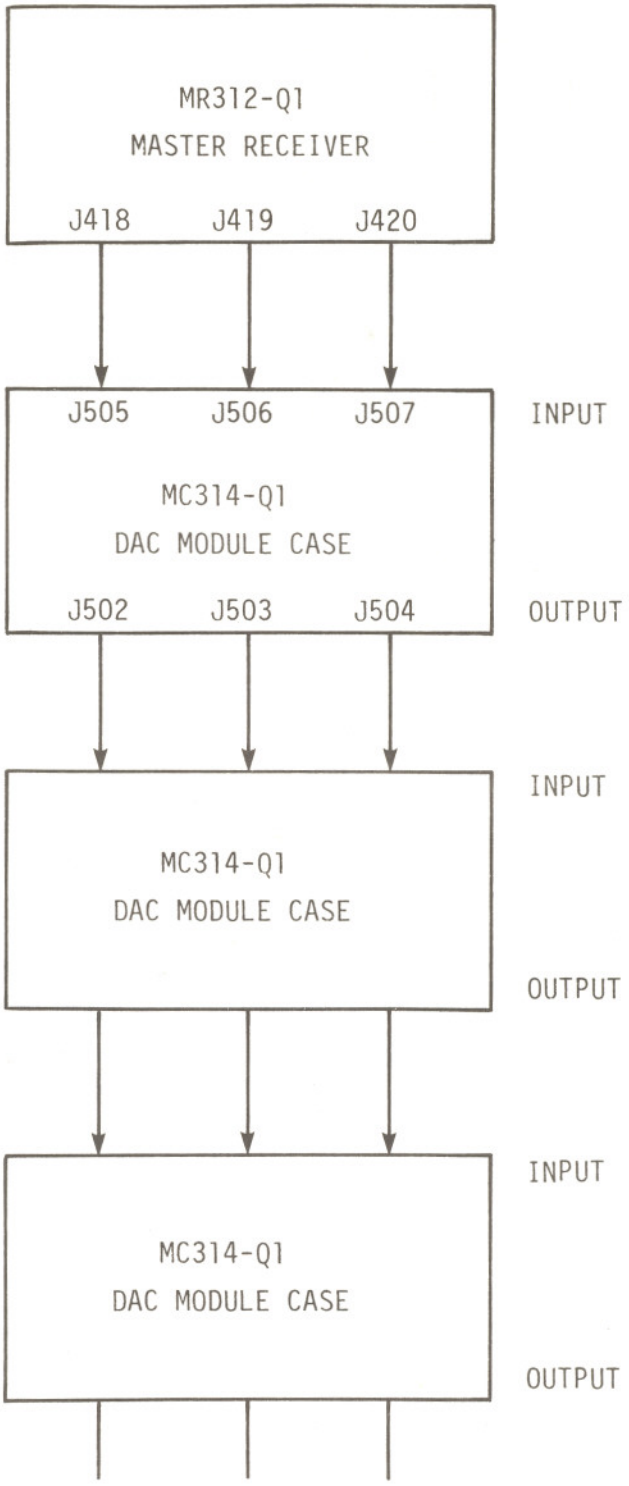


Figure 3-4. Connection of MC314-Q1 Module Cases to Master Receiver.

Table 3-7. J419 Connector Playback Data/DAC.

(37 PIN - FEMALE)				
Pin #	Signal Name	Hi/Lo	Function	Activated By
1	RDPCM1	L	Link 1 Recorded Data	Recorder
2	RDPCM1	H	Link 1 Recorded Data	Recorder
3	RDPCM2	L	Link 2 Recorded Data	Recorder
4	RDPCM2	H	Link 2 Recorded Data	Recorder
5	RDPCM3	L	Link 3 Recorded Data	Recorder
6	RDPCM3	H	Link 3 Recorded Data	Recorder
7	RDPCM4	L	Link 4 Recorded Data	Recorder
8	RDPCM4	H	Link 4 Recorded Data	Recorder
9	RDPCM5	L	Link 5 Recorded Data	Recorder
10	RDPCM5	H	Link 5 Recorded Data	Recorder
11	RDPCM6	L	Link 6 Recorded Data	Recorder
12	RDPCM6	H	Link 6 Recorded Data	Recorder
13	RDPCM7	L	Link 7 Recorded Data	Recorder
14	RDPCM7	H	Link 7 Recorded Data	Recorder
15	RDPCM8	L	Link 8 Recorded Data	Recorder
16	RDPCM8	H	Link 8 Recorded Data	Recorder
17	RDPCM9	L	Link 9 Recorded Data	Recorder
18	RDPCM9	H	Link 9 Recorded Data	Recorder
19	GND		Signal Ground	
20	RDPCM10	L	Link 10 Recorded Data	Recorder
21	RDPCM10	L	Link 10 Recorded Data	Recorder
22	RDPCM11	H	Link 11 Recorded Data	Recorder
23	RDPCM11	L	Link 11 Recorded Data	Recorder
24	RDPCM12	H	Link 12 Recorded Data	Recorder
25	RDPCM12	L	Link 12 Recorded Data	Recorder
26	RDPCM13	H	Link 13 Recorded Data	Recorder
27	RDPCM13	L	Link 13 Recorded Data	Recorder
28	RDPCM14	H	Link 14 Recorded Data	Recorder
29	RDPCM14	L	Link 14 Recorded Data	Recorder
30	RDPCM15	H	Link 15 Recorded Data	Recorder
31	RDPCM15	L	Link 15 Recorded Data	Recorder
32	RDPCM16	H	Link 16 Recorded Data	Recorder
33	RDPCM16	L	Link 16 Recorded Data	Recorder
34			Not Assigned	
35			Not Assigned	
36			Not Assigned	
37			Not Assigned	

3-39. Connect up to 37 wires to a mating connector and connect to the MC314-Q1 DAC Module Case. If more than one MC314-Q1 DAC Module Case is used with the system, they can be serially connected together as shown in Figure 3-4.

3-40. J418 DAC LIVE DATA Connections. The J418 is a 37-pin type "D" female connector which provides the same data input functions to the DACs as the JD-2 connector except that it transmits "live" data. Table 3-8 gives the pin assignments.

3-41. Connect up to 37 wires to a mating connector and connect to the MC314-Q1 DAC Module Case. If more than one MC314-Q1 DAC Module Case is used with the system, it can be serially connected together as shown in Figure 3-4.

Table 3-8. J418 Connector Live Data.

(37 PIN - FEMALE)				
Pin #	Signal Name	Hi/Lo	Function	Activated By
1	RDLV1	L	Link 1 Live Data	Receiver Card #1
2	RDLV1	H	Link 1 Live Data	Receiver Card #1
3	RDLV2	L	Link 2 Live Data	Receiver Card #2
4	RDLV2	H	Link 2 Live Data	Receiver Card #2
5	RDLV3	L	Link 3 Live Data	Receiver Card #3
6	RDLV3	H	Link 3 Live Data	Receiver Card #3
7	RDLV4	L	Link 4 Live Data	Receiver Card #4
8	RDLV4	H	Link 4 Live Data	Receiver Card #4
9	RDLV5	L	Link 5 Live Data	Receiver Card #5
10	RDLV5	H	Link 5 Live Data	Receiver Card #5
11	RDLV6	L	Link 5 Live Data	Receiver Card #6
12	RDLV6	H	Link 6 Live Data	Receiver Card #6
13	RDLV7	L	Link 7 Live Data	Receiver Card #7
14	RDLV7	H	Link 7 Live Data	Receiver Card #7
15	RDLV8	L	Link 8 Live Data	Receiver Card #8
16	RDLV8	H	Link 8 Live Data	Receiver Card #8
17	RDLV9	L	Link 8 Live Data	Receiver Card #9
18	RDLV9	H	Link 9 Live Data	Receiver Card #9
19	GND		Signal Ground	
20	RDLV10	H	Link 10 Live Data	Receiver Card #10
21	RDLV10	L	Link 10 Live Data	Receiver Card #10
22	RDLV11	H	Link 11 Live Data	Receiver Card #11
23	RDLV11	L	Link 11 Live Data	Receiver Card #11
24	RDLV12	H	Link 12 Live Data	Receiver Card #12
25	RDLV12	L	Link 12 Live Data	Receiver Card #12
26	RDLV13	H	Link 13 Live Data	Receiver Card #13
27	RDLV13	L	Link 13 Live Data	Receiver Card #13
28	RDLV14	H	Link 14 Live Data	Receiver Card #14
29	RDLV14	L	Link 14 Live Data	Receiver Card #14
30	RDLV15	H	Link 15 Live Data	Receiver Card #15
31	RDLV15	L	Link 15 Live Data	Receiver Card #15
32	RDLV16	H	Link 16 Live Data	Receiver Card #16
33	RDLV16	H	Link 16 Live Data	Receiver Card #16
34			Not Assigned	
35			Not Assigned	
36			Not Assigned	
37			Not Assigned	

SECTION IV
OPERATION

4-1. PRELIMINARY CHECKOUT.

After the system has been installed as described in Section III, apply power by placing the POWER Switch on the Model PS320-Q1 Power Supply to the ON position. The green ON indicator in the front panel of the Power Supply will illuminate indicating power is being applied. If light does not illuminate, first check that the 120 Vac line has been properly connected to the Master Receiver. Next check that the fuse in the Power Supply is operational and is the correct rating. If fuse is blown, replace with a new one. If fuse continues to blow, replace Power Supply before returning system to service. See separate manual on the PS320-Q1 Power Supply.

4-2. Next check that all ERROR lights on the DR317-Receiver Cards are extinguished and ACTIVE SUBLINK channel number lights are illuminated (green) according to the sublink number set on the DR317-Q1 Cards. If any ERROR lights are lit, shut system down and remove the Receiver Cards which have error lights lit, and check that the DIP Switches for the sublinks have been properly set (see Paragraph 3-10). If switches have been properly set, check electrical (or fiber optic) cabling from the Multiplexer or Submultiplexers to the Master Receiver to make sure that cables are properly connected (see Paragraph 3-16). If cables are properly connected and error lights still remain lit, troubleshoot the entire system by first interchanging Receiver Cards, then making sure link and sublink switches in the Remote Multiplexers are properly set and electrical connections properly made. (See individual manuals on the Multiplexer and Submultiplexer for details.)

4-3. Additional checks can be made at the DA313-Q1 Digital-to-Analog Converter Module (if installed in the system). See Paragraph 4-4 for details.

4-4. TESTING WITH INTERNAL DIGITAL-TO-ANALOG CONVERTER.

Individual channels, links, and sublinks can be tested by means of the DA313-Q1 Digital-to-Analog Converter, when installed in the Master Receiver. This is accomplished as follows:

A. Set the LOCAL/REMOTE Switch on the DA313-Q1 to the LOCAL position. Switch should always be in this position since the DA313-Q1 will not work in the REMOTE mode when installed in the Master Receiver. (Switch is ignored in TG319-Q1 software.)

B. Set the LIVE/PCM Switch to the proper position; LIVE if testing data directly, or PCM if testing recorded signals from the PCM Recorder.

C. Select the desired LINK, SUBLINK, and CHANNEL number by exercising the pushbutton switches directly below the LED windows for the LINK, SUBLINK, and CHANNEL number indicators. Numbers will go higher or lower depending on whether the upper or lower pushbutton switch is depressed.

D. Connect a DC voltmeter, pen recorder, strip chart recorder or oscillograph betwen the TP+ and TP- connection on the DA313-Q1. Agreement of a known voltage of a particular channel indicates that the selected LINK, SUBLINK and CHANNEL is operating properly, and live data is coming through the system.

E. If the selected data source is not active (that is, not being updated repeated) the identification display will blink to alert the equipment operator. Additionally, if data updates are interrupted, the analog output signal will be driven off-scale, the equivalent of $\approx$112.5% of positive full scale range.

F. Consult the DA313-Q1 Operating Manual for complete operation and maintenance instructions. Normally, only the controls mentioned here apply to the DA313-Q1 when used in the Master Receiver.

4-5. OPERATING PROCEDURE.

Operating procedures for the RC321 Tape Control Modules, DA313-Q1 Digital-to-Analog Converter, and TG319-Q1 Time Code Generator are located in separate manuals.

SECTION V
MAINTENANCE

5-1. TROUBLESHOOTING.

Table 5-1 gives a general troubleshooting guide to the MR312-Q1 Master Receiver while observing indications on the Module Case only. This section on maintenance covers the MR312-Q1 Master Receiver Case, the DR317-Q1 Receiver Input Card, the CS348-Q1 Control Sequencer Card and the AG351-Q1 Address Generator Card. Maintenance on other circuit boards and modules of the Master Receiver are located in separate manuals.

5-2. The easiest method of determining which component of the MR312 Master Receiver is defective is by substituting a circuit board (or module) known to be good with one suspected of being defective. This logically will pinpoint the trouble to a particular circuit board which can be replaced and repaired at a later date.

5-3. MAINTENANCE PROCEDURE.

To further isolate a trouble within the MR312-Q1 itself or on one of the circuit boards, the following wiring diagrams and schematics are included: Figure 5-1 is the Master Receiver Wiring Diagram. Figure 5-2 is the Schematic Diagram for the DR317-Q1 Receiver Input Card A and Figure 5-3 is the Receiver Input Card B. Figure 5-4 is the Schematic Diagram for the CS348-Q1 Control Sequencer Card, and Figure 5-5 is the AG351-Q1 Address Generator Card.

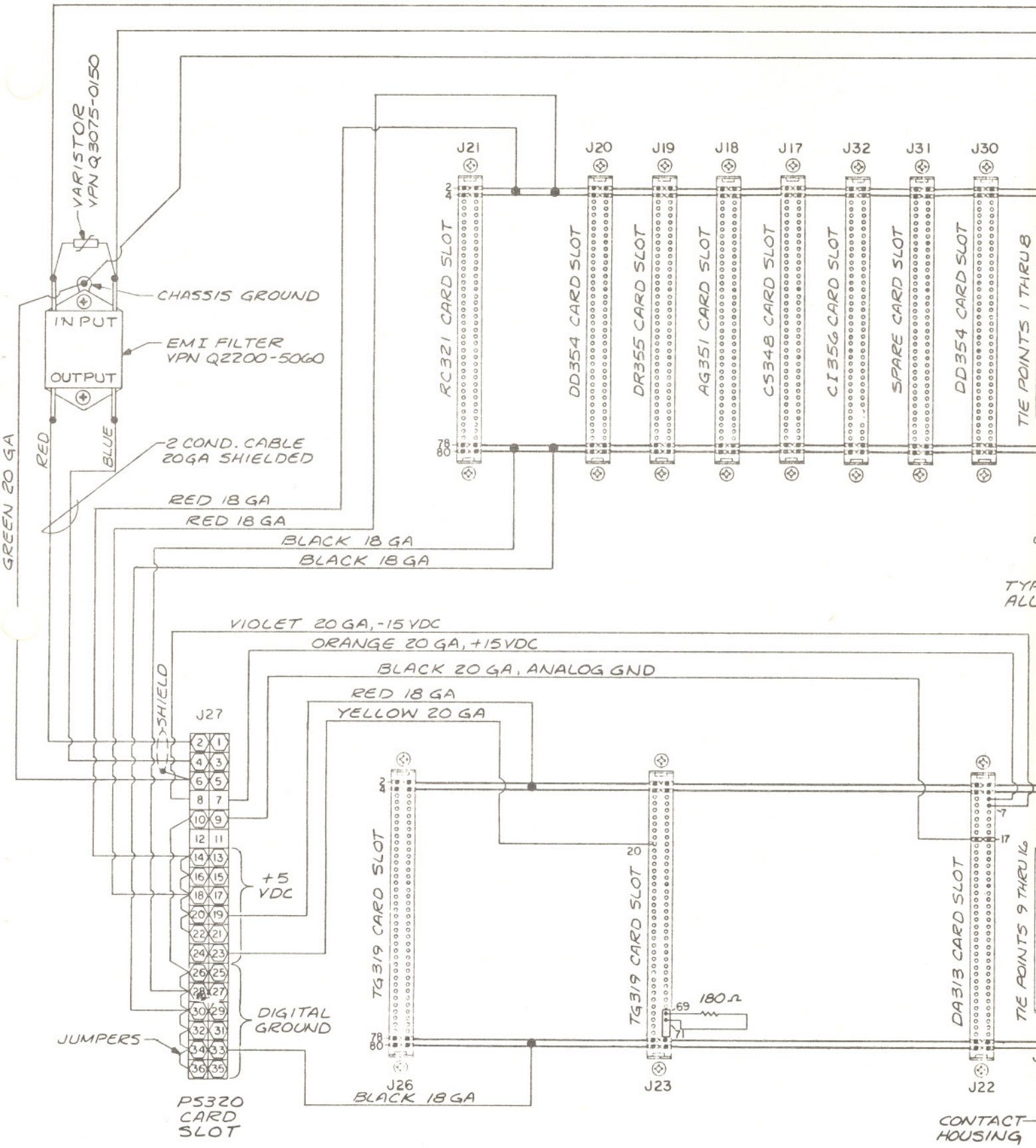
5-4. To aid in location of parts on the various circuit boards, the following assembly drawings are included: Figure 5-6 is the DR317-Q1 Receiver Input Card A and Figure 5-7 is the Receiver Input Card B. Figure 5-8 is the CS348-Q1 Control Sequencer Circuit Board Assembly, and Figure 5-9 is the AG351-Q1 Address Generator Circuit Board Assembly.

Table 5-1. Troubleshooting Chart.

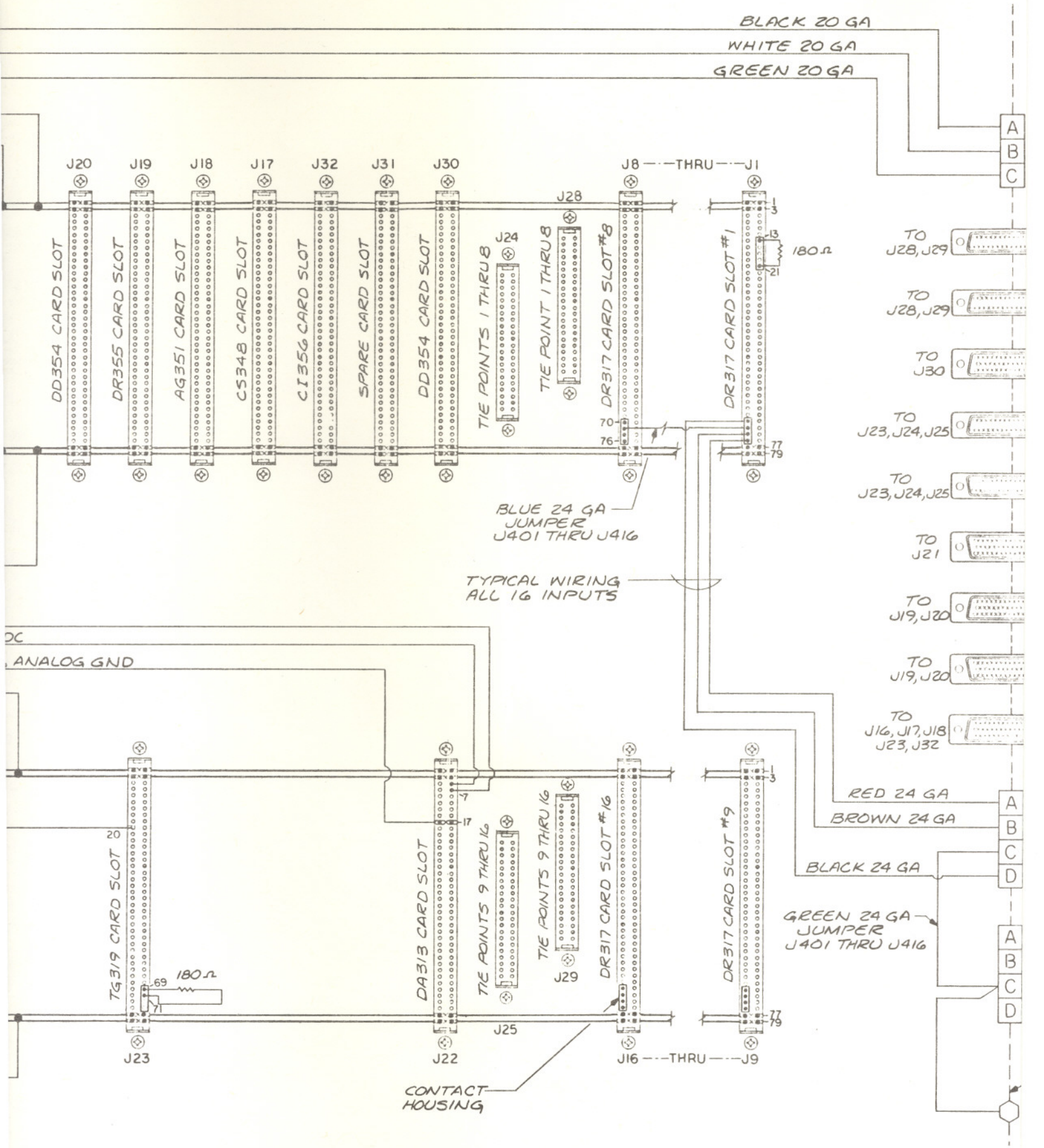
TROUBLE	POSSIBLE CAUSE	REMEDY
1A1. No Power to system.	1B1. Power source not connected.	1C1. Check that 115 Vac power is connected to system.
	1B2. Defective PS320-Q1 Power Supply.	Check that Power Supply POWER is ON and indicator light is lit. If not, check for blown fuse in Power Supply. Replace fuse if defective. Check for defective Power Supply Module. See individual manual on Power Supply.
DR317-Q1 RECEIVER CARD		
2A1. One or more error lights lit.	2B1. Receiver Card DIP Switches improperly set.	2C1. Reset DIP Switches as described in Paragraph 3-10.
	2B2. Fiber optics or electrical cables improperly connected to Master Receiver.	2C2. Reconnect cables as described in Paragraph 3-16.
	2B3. Malfunction in the Multiplexer or Submultiplexer feeding the Master Receiver.	2C3. Troubleshoot entire system making sure LINK and SUBLINK Switches on the Multiplexers and Submultiplexers are properly set. Check that all electrical or fiber optic connections are properly made (see individual manuals on Multiplexers and Submultiplexers for details).
	2B4. OPTICAL/DIFF Switch improperly set.	2C4. Check that Switch is properly set and reset as necessary. See Paragraph 3-10 for details.

Table 5-1. Troubleshooting Chart (Continued).

TROUBLE	POSSIBLE CAUSE	REMEDY
	2B5. Dirt on end of fiber optic cable (if used).	2C5. Check end of fiber optic cable and clean if necessary.
3A1. No active SUB-LINK channel number lit.	3B1. Same as 1B1, 1B2, 2B1, 2B2, or 2B3.	3C1. Same as 1C1, 1C2, 2C1, 2C2, or 2C3.
	3B2. Board not making good electrical contact with board edge connector in module case.	3C2. Make sure circuit board is pushed all the way back into case and is making good electrical contact with board edge connector.
4A1. Signal being received but no computer interface.	4B1. Defective circuit board in Receiver Programmer Card set.	4C1. Using board substitution method, check the Differential Driver Circuit Board, Differential Receiver Circuit Board, Address Generator Circuit Board, Control Sequencer Circuit Board, and Computer Interface Circuit Board. Replace defective circuit board.
	4B2. Defective host computer.	4C2. Troubleshoot host computer according to the computer manual. Check interconnecting wires between computer and Master Receiver and repair or replace as necessary.



1. ⬡ OR ⊶ INDICATES CONNECTOR PINS THAT ARE BO



INDICATES CONNECTOR PINS THAT ARE BUSSED TOGETHER.

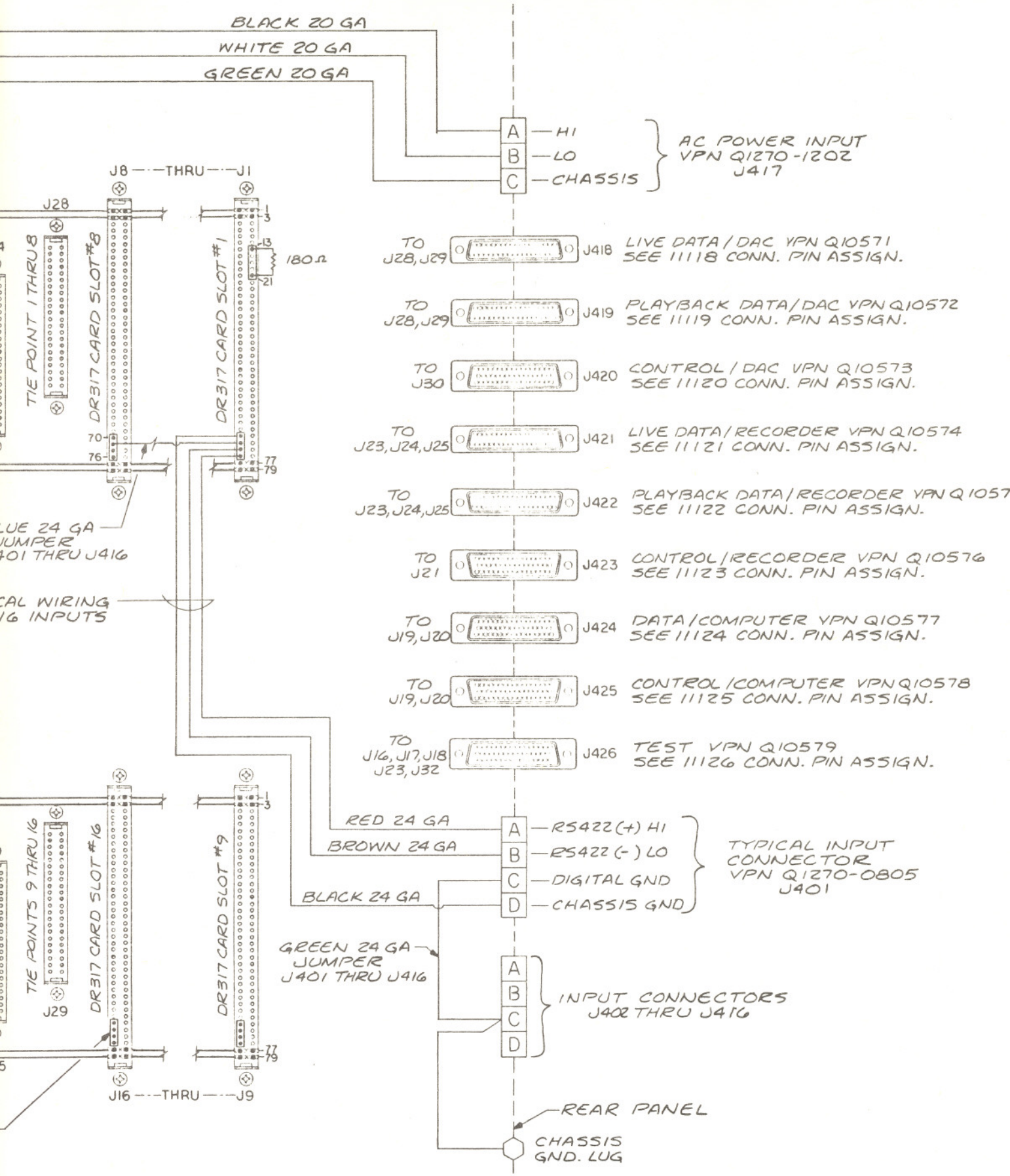
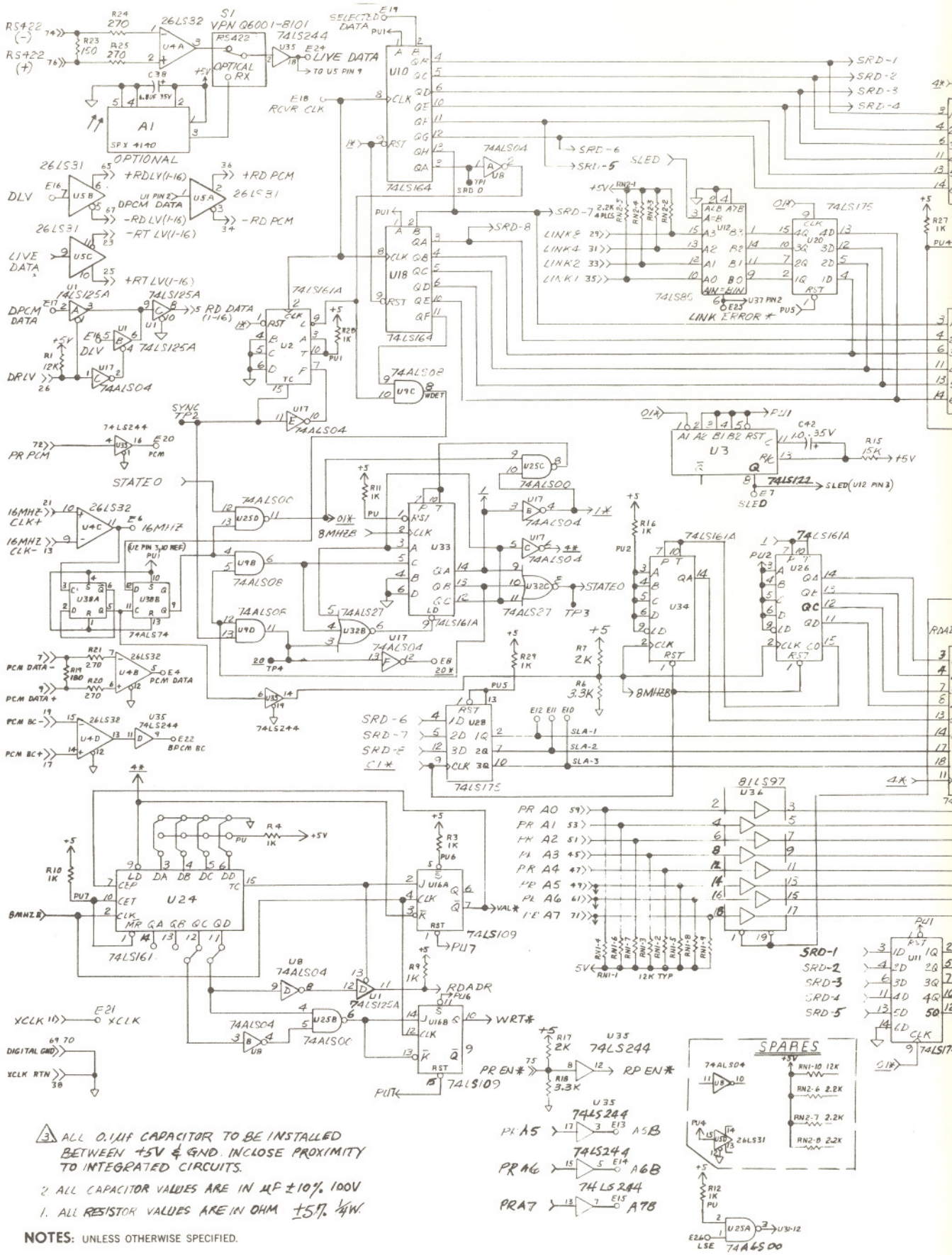


Figure 5-1. Master Receiver Wiring Diagram.


RS422 (-)
RS422 (+)
26LS32
S1 VPN Q6001-8101
74LS244
LIVE DATA
SELECTED DATA
RCVR CLK
OPTIONAL
26LS31
DLV
DPCM DATA
LIVE DATA
74LS125A
74LS164
74LS161A
74LS175
74LS86
74ALS04
74ALS08
74ALS00
74ALS27
74LS74
74LS109
74LS161
74LS97
74LS122
LINK ERROR *
SLED
SRD-1
SRD-2
SRD-3
SRD-4
SRD-5
SRD-6
SRD-7
SRD-8
PR PCM
STATE0
16MHZ CLK+
16MHZ CLK-
8MHZB
1X
4X
PCM DATA -
PCM DATA +
PCM BC -
PCM BC +
YCLK
DIGITAL GND
YCLK RTN
RDADR
WRT*
PR EN*
RP EN*
SPARES
ALL 0.1uf CAPACITOR TO BE INSTALLED BETWEEN +5V & GND. INCLOSE PROXIMITY TO INTEGRATED CIRCUITS.
ALL CAPACITOR VALUES ARE IN uF ±10%, 100V
ALL RESISTOR VALUES ARE IN OHM ±5%, ¼W.
NOTES: UNLESS OTHERWISE SPECIFIED.

SRD-1
SRD-2
SRD-3
SRD-4
SRD-5
SRD-6
SRD-7
SRD-8
SLED
LINK ERROR *
WRT *
RPEN *
RDADR
STATE0
8MHZ
4X
1X
VAL *
PR A0
PR A1
PR A2
PR A3
PR A4
PR A5
PR A6
PR A7
SPARES
74LS174
74LS175
74LS161A
74LS244
74LS374
74LS245
74LS85
74LS109
74LS27
74LS04
74LS38
74LS08
74LS32
74LS00
5101
+5VDC
REVERSE VOLTAGE PROTECTION
CR1 IN5820
GND
DI-13

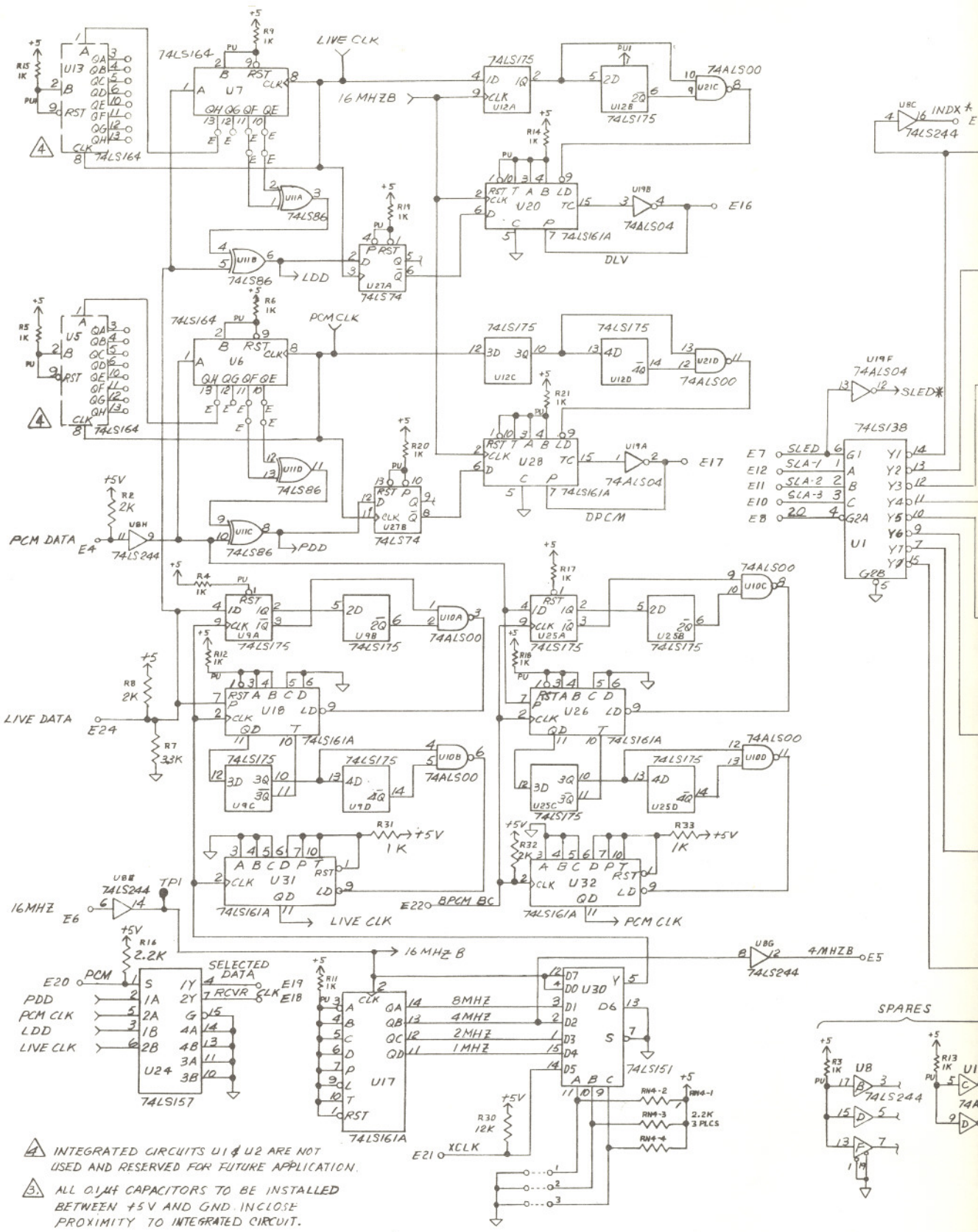
Figur

REVISIONS			
SYM	DESCRIPTION	DATE	APPROVED

CABLE INTERCONNECT CHART	
CABLE WIRE	SIGNAL NAME
E1	GROUND
E2	GROUND
E3	INDX *
E4	PCM DATA
E5	4 , , 3
E6	16 MHZ
E7	SLED
E8	20 *
E9	GSLE *
E10	SLA-3
E11	SLA-2
E12	SLA-1
E13	A5B
E14	A6B
E15	A7B
E16	ULV
E17	DPCM
E18	RCVR CLK
E19	SELECTED DATA
E20	PCM
E21	XCLK
E22	BPCM BC
E23	———
E24	LIVE DATA
E25	LINK ERROR *
E26	LSE
E27	———
E28	LSER
E29	+5VDC
E30	+5VDC

INTEGRATED CIRCUIT CHART			
REF. DES.	TYPE	V_{CC} PIN NO	GND PIN NO
U7, 15, 23, 31, 37	74LS38	14	7
U12, 19, 27	74LS85	16	8
U3	74LS122	14	7
U2, 24, 26, 33, 34	74LS161A	16	8
U10, 18	74LS164	14	7
U11, 13, 21	74LS174	16	8
U20, 28	74LS175	16	8
U29	74LS374	20	10
U36	81LS97	20	10
U25	74ALS00	14	7
U8, 17	74ALS04	14	7
U9	74ALS08	14	7
U32	74ALS27	14	7
U6, 14, 22, 30	5101-1	22	8
U16	74LS109	16	8
U5	26LS31	16	8
U4	26LS32	16	8
U1	74LS125	14	7
U35	74LS244	20	10
U38	74LS74	14	7

Figure 5-2. DR317-Q1 Receiver Input Card A, Schematic Diagram.



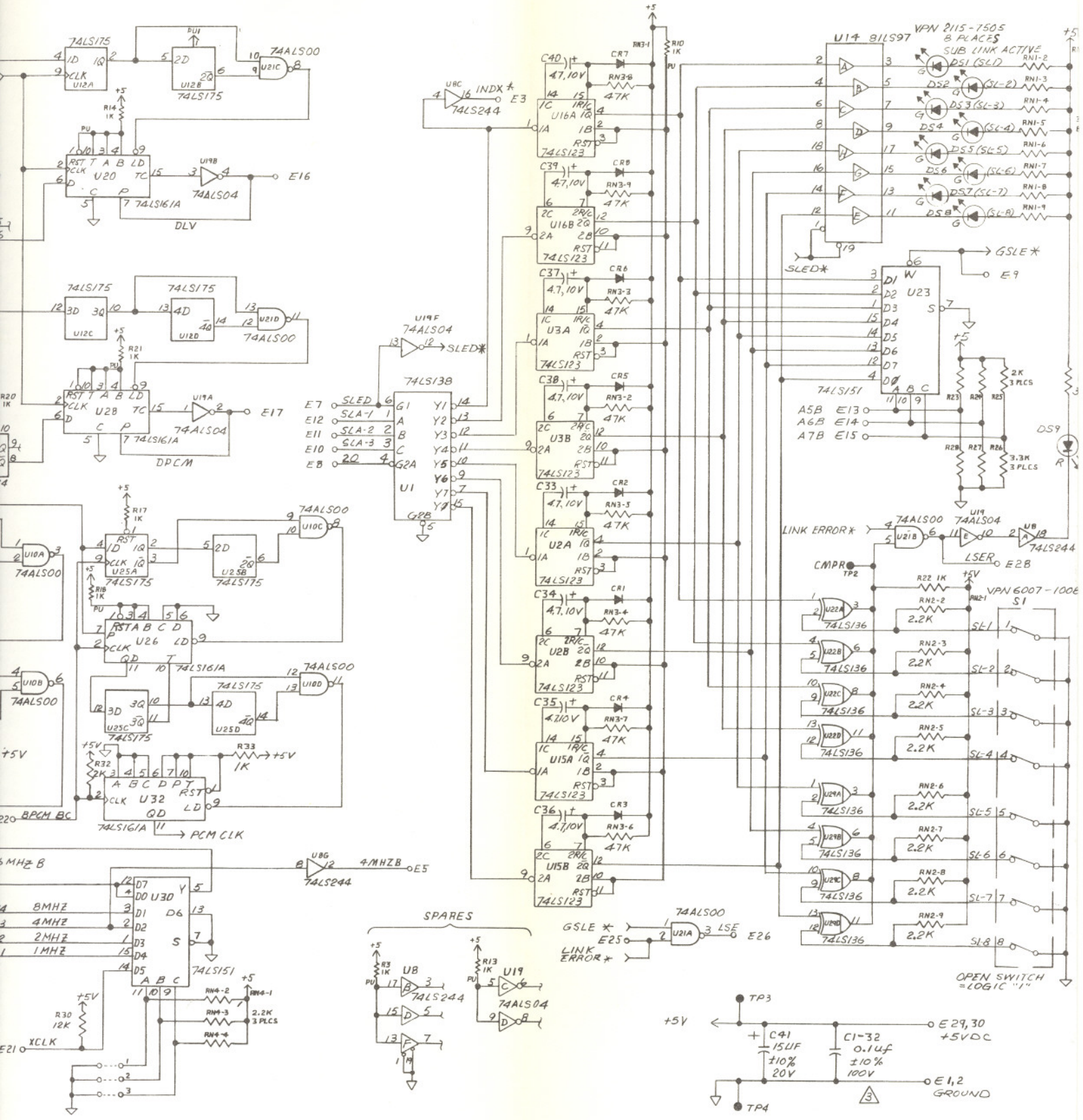
4. INTEGRATED CIRCUITS U1 & U2 ARE NOT USED AND RESERVED FOR FUTURE APPLICATION.

3. ALL 0.1μf CAPACITORS TO BE INSTALLED BETWEEN +5V AND GND. INCLOSE PROXIMITY TO INTEGRATED CIRCUIT.

2. ALL CAPACITOR VALUES ARE IN MICROFARADS ± 10%, 100V.

1. ALL RESISTOR VALUES ARE IN OHMS ±5%. 1/4 W.

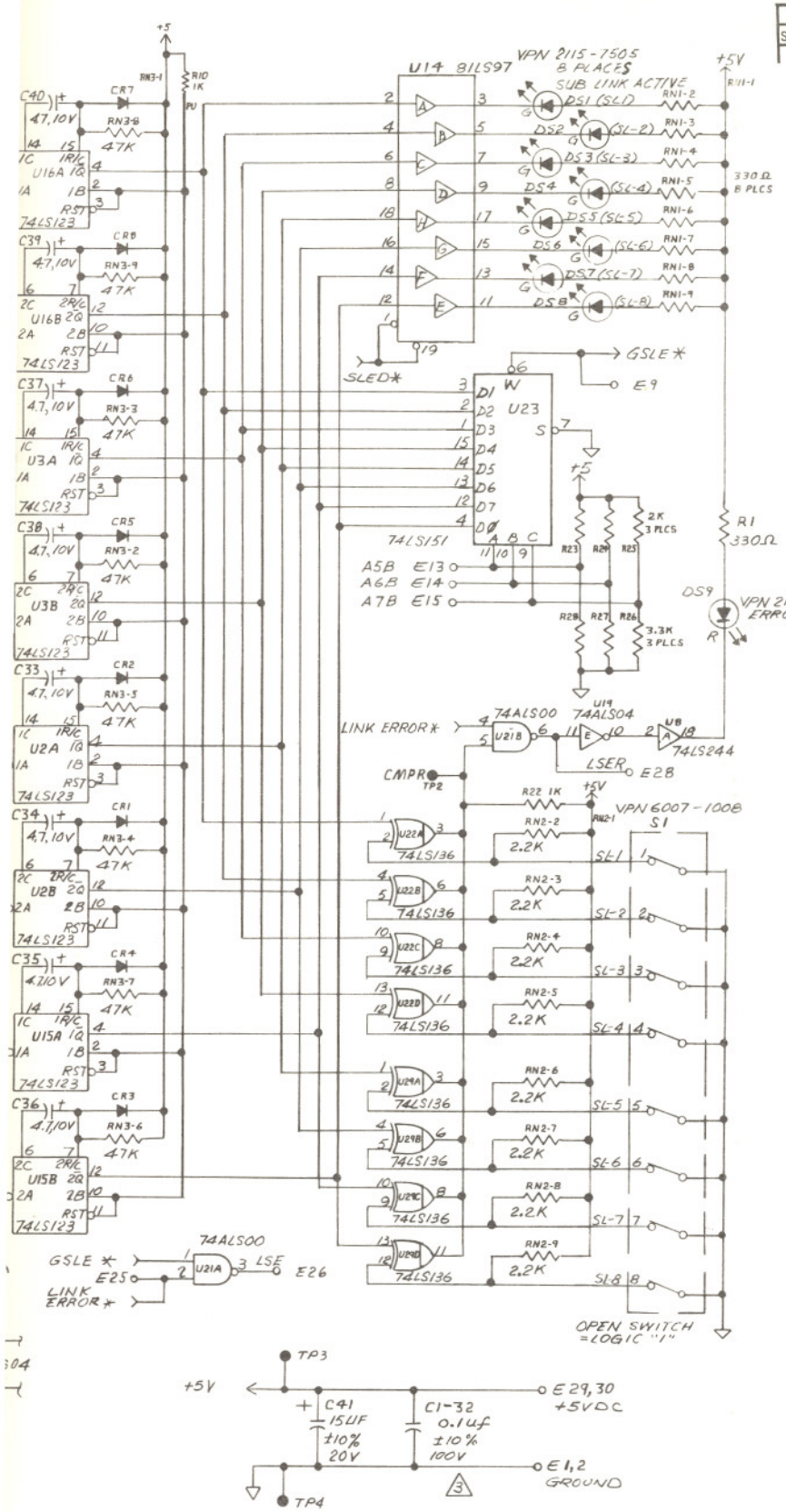
NOTES: UNLESS OTHERWISE SPECIFIED.


74LS175
74ALS00
74LS161A
74ALS04
74LS138
74LS123
74LS151
74LS136
74LS244
74LS157
DLV
DPCM
PCM CLK
SPARES
VPN 2115-7505
8 PLACES
SUB LINK ACTIVE
VPN 6007-1006
OPEN SWITCH
=LOGIC "1"
+5VDC
GROUND
XCLK
LINK ERROR*
GSLE*
SLED*
LSER
CMPR
INDX*
4MHZB
8MHZB
4MHZ
2MHZ
1MHZ
BPCM BC
C41 15UF ±10% 20V
C1-32 0.1uf ±10% 100V

Figur

10264

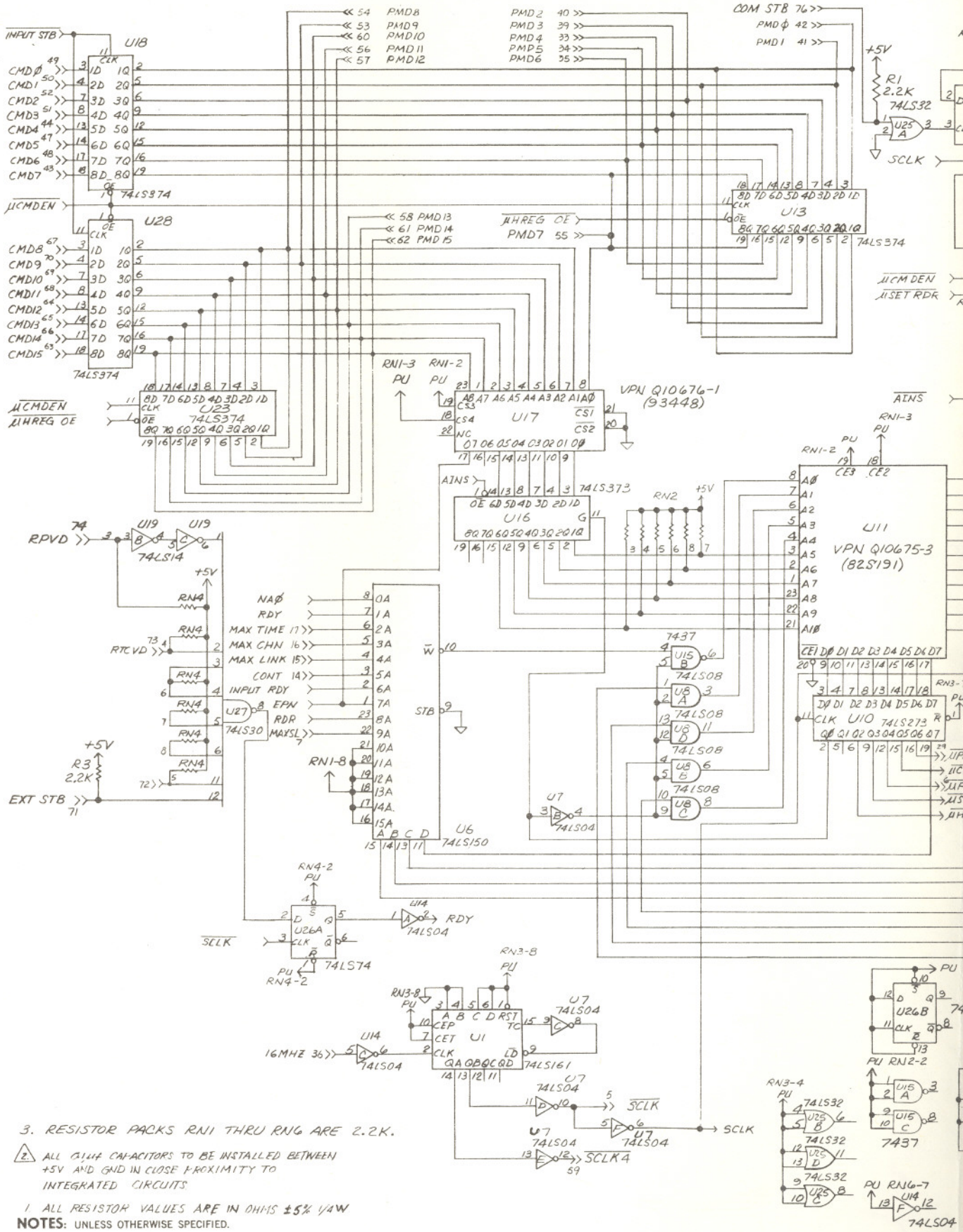
REVISIONS			
SYM	DESCRIPTION	DATE	APPROVED



CABLE INTERCONNECT CHART		
	CABLE WIRE	SIGNAL NAME
	E1	GROUND
	E2	GROUND
	E3	INDX *
	E4	PCM DATA
	E5	4 MHZB
	E6	16 MHZ
	E7	SLED
	E8	20*
	E9	GSLE *
	E10	SLA-3
	E11	SLA-2
	E12	SLA-1
	E13	A5B
	E14	A6B
	E15	A7B
	E16	DLV
	E17	DPCM
	E18	RCVR CLK
	E19	SELECTED DATA
	E20	PCM
	E21	XCLK
	E22	BPCM BC
	E23	———
	E24	LIVE DATA
	E25	LINK ERROR *
	E26	LSE
	E27	———
	E28	LSER
	E29	+5VDC
	E30	+5VDC

INTEGRATED CIRCUIT CHART			
REF DES	TYPE	VCC PIN No	GND PIN No
U11	74LS86	14	7
U2, 3, 15, 16	74LS123	16	8
U22, 29	74LS136	14	7
U1	74LS138	16	8
U23, 30	74LS151	16	8
U24	74LS157	16	8
U17, 18, 20, 26, 28, 31, 32	74LS161A	16	8
U5, 6, 7, 13	74LS164	14	7
U9, 12, 25	74LS175	16	8
U8	74LS244	20	10
U10, 21	74ALS00	14	7
U19	74ALS04	14	7
U14	81LS97	20	10
U27	74ALS74	14	7
U4	SPARE	16	8

Figure 5-3. DR317-Q1 Receiver Input Card B, Schematic Diagram.

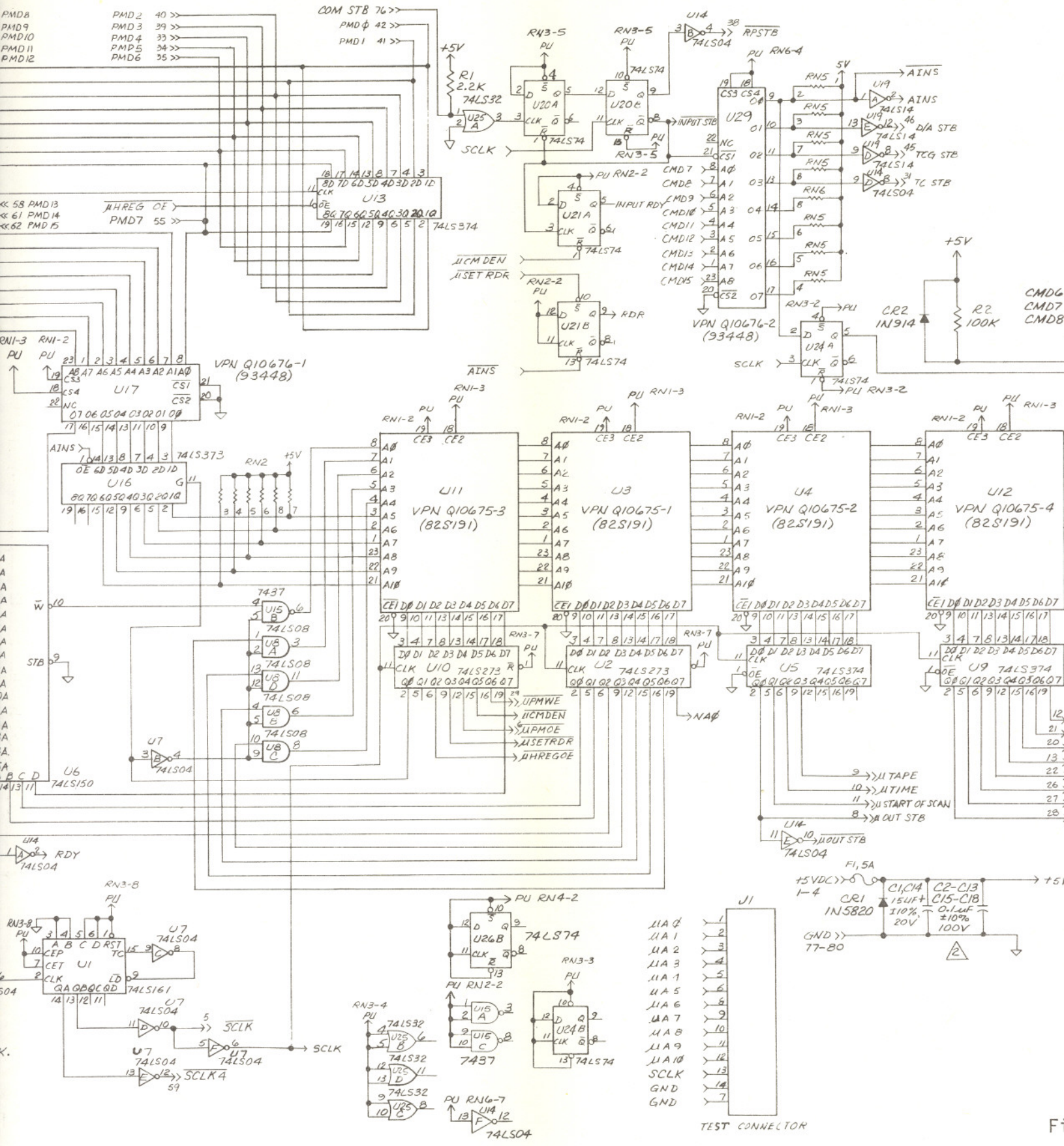


3. RESISTOR PACKS RN1 THRU RN6 ARE 2.2K.

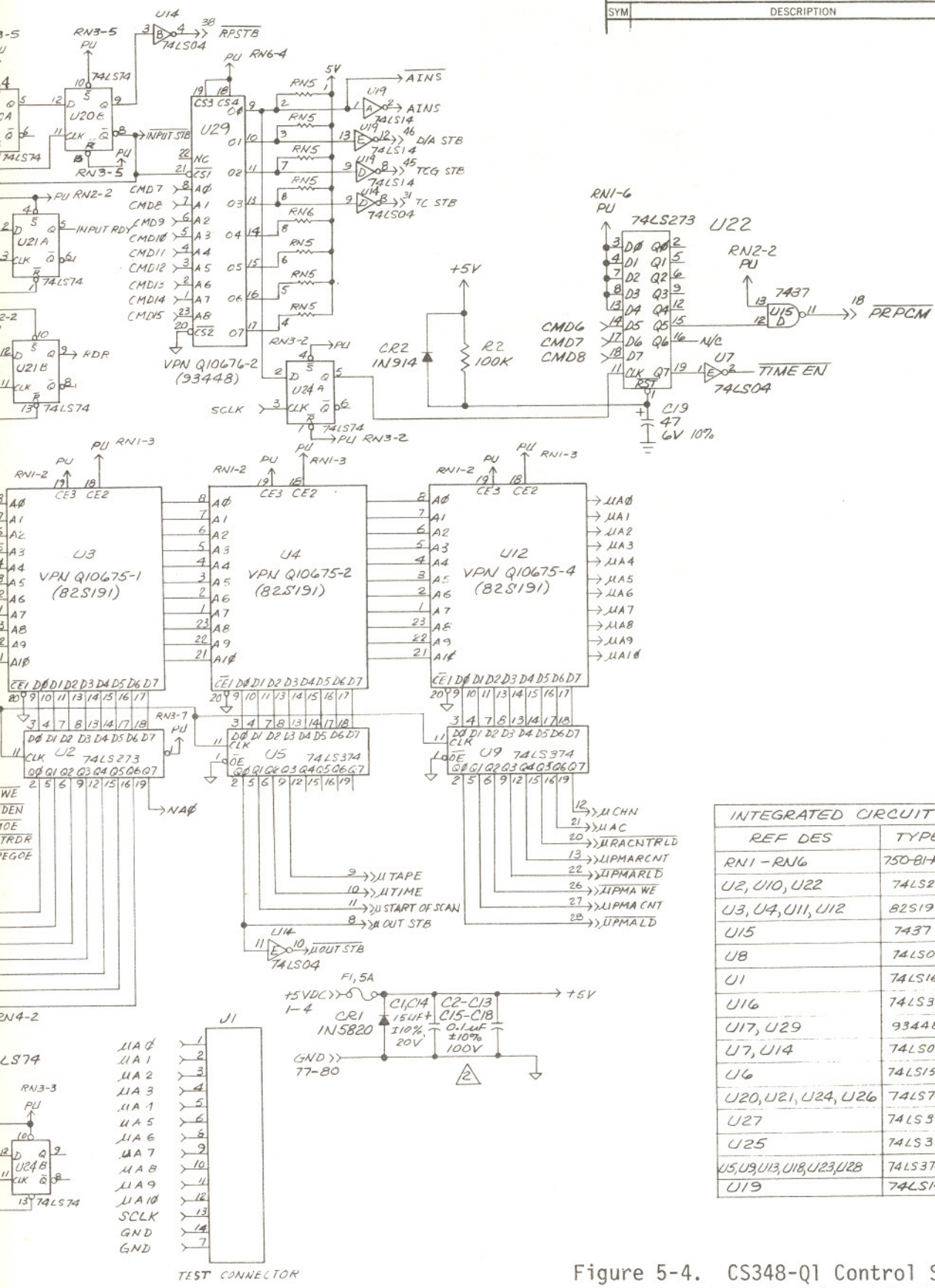
2. ALL CHIP CAPACITORS TO BE INSTALLED BETWEEN +5V AND GND IN CLOSE PROXIMITY TO INTEGRATED CIRCUITS.

1. ALL RESISTOR VALUES ARE IN OHMS ±5% 1/4W

NOTES: UNLESS OTHERWISE SPECIFIED.

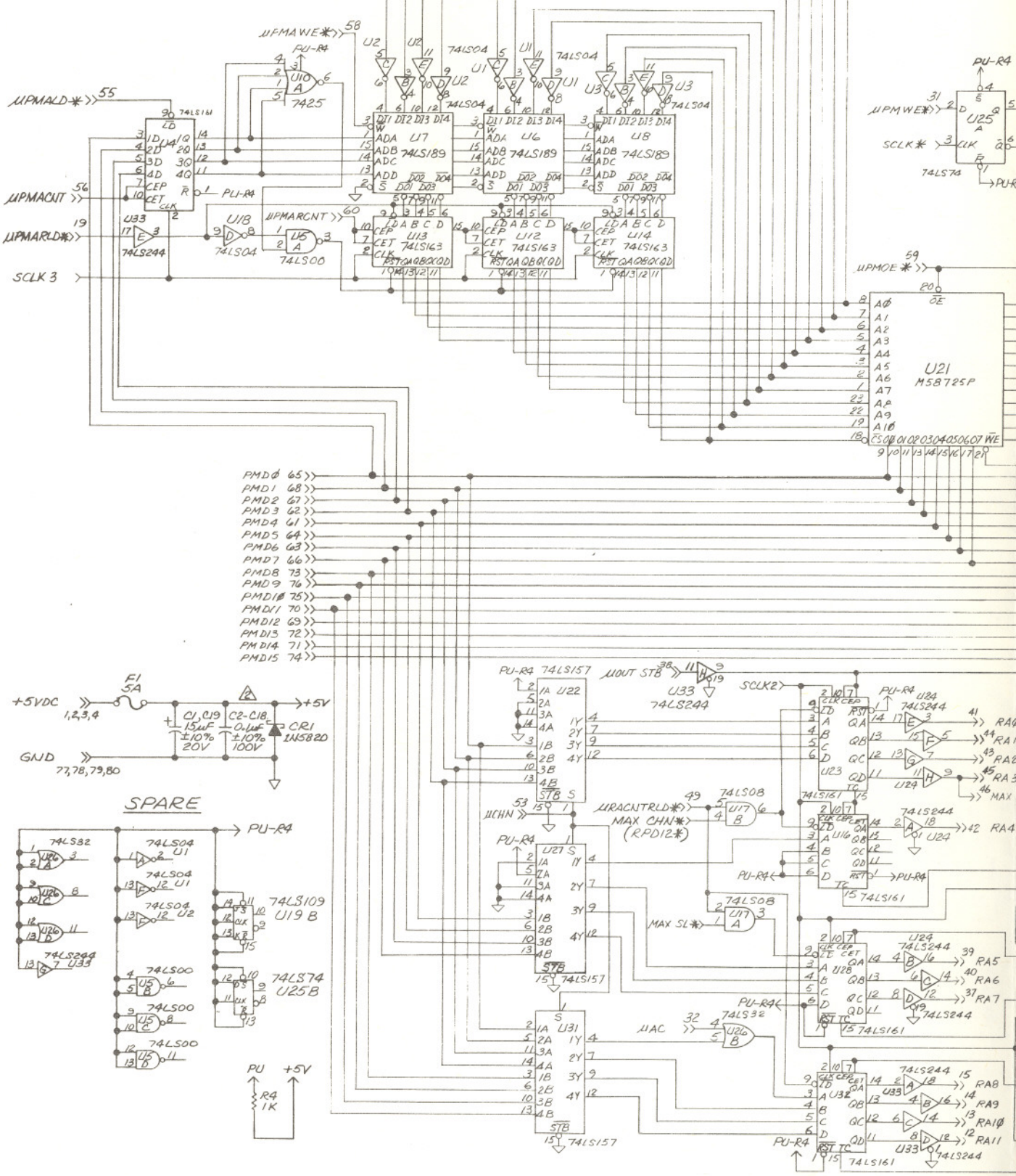

PMD8
PMD9
PMD10
PMD11
PMD12
PMD2 40
PMD3 39
PMD4 33
PMD5 34
PMD6 35
COM STB 76
PMDØ 42
PMD1 41
+5V
R1
2.2K
74LS32
SCLK
RN3-5
U20A
U20E
74LS74
U14
74LS04
RPSTB
INPUT STB
RN3-5
RN6-4
U29
CMD7
CMD8
CMD9
CMD10
CMD11
CMD12
CMD13
CMD14
CMD15
VPN Q10676-2
(93448)
RN5
U19
AINS
D/A STB
TCG STB
TC STB
74LS14
RN6
RN2-2
U21A
INPUT RDY
U13
74LS374
58 PMD13
61 PMD14
62 PMD15
μHREG OE
PMD7 55
μCMDEN
μSETRDR
U21B
RDY
RN3-2
U24A
CR2
IN914
R2
100K
CMD6
CMD7
CMD8
RNI-3
RNI-2
U17
VPN Q10676-1
(93448)
74LS373
U16
RN2
U11
VPN Q10675-3
(82S191)
U3
VPN Q10675-1
(82S191)
U4
VPN Q10675-2
(82S191)
U12
VPN Q10675-4
(82S191)
7437
74LS08
U6
74LS150
U7
74LS04
U10
74LS273
U2
74LS273
U5
74LS374
U9
74LS374
μPMWE
μCMDEN
μPMOE
μSETRDR
μHREGOE
NAØ
μTAPE
μTIME
μSTART OF SCAN
μOUT STB
RDY
RN3-8
U1
74LS161
SCLK
SCLK4
U26B
74LS74
U24B
74LS374
7437
74LS32
RN6-7
J1
TEST CONNECTOR
+5VDC
1-4
F1, 5A
CR1
IN5820
C1,C14
15μF+
110%,
20V
C2-C13
C15-C18
0.1μF
±10%
100V
GND
77-80

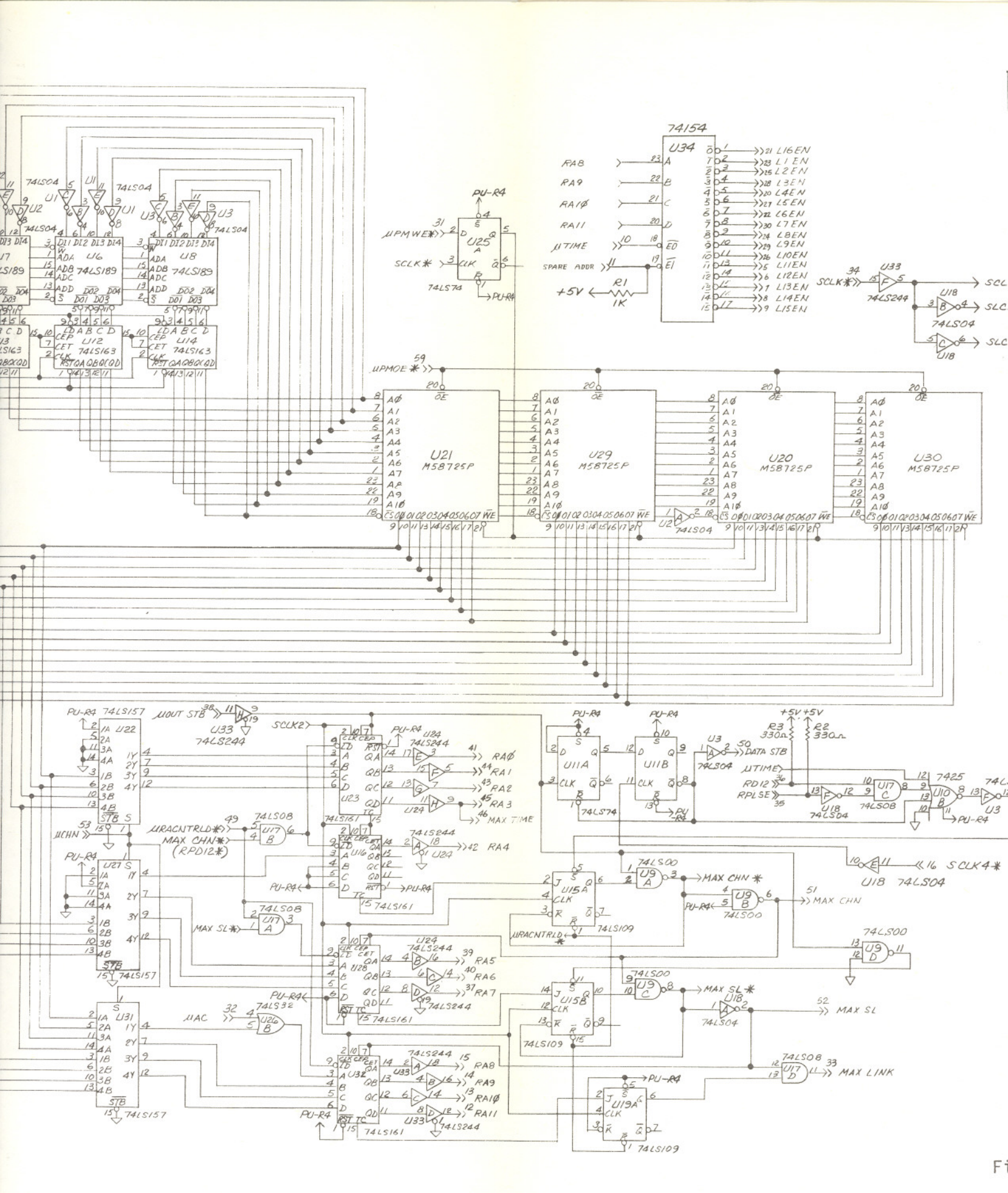
REVISIONS			
SYM	DESCRIPTION	DATE	APPROVED



INTEGRATED CIRCUIT CHART			
REF DES	TYPE	Vcc	GND
RN1 - RN6	750-81-R22K	1	—
U2, U10, U22	74LS273	20	10
U3, U4, U11, U12	82S191	24	12
U15	7437	14	7
U8	74LS08	14	7
U1	74LS161	16	8
U16	74LS373	20	10
U17, U29	93448	24	12
U7, U14	74LS04	14	7
U6	74LS150	24	12
U20, U21, U24, U26	74LS74	14	7
U27	74LS30	14	7
U25	74LS32	14	7
U5, U9, U13, U18, U23, U28	74LS374	20	10
U19	74LS14	14	7

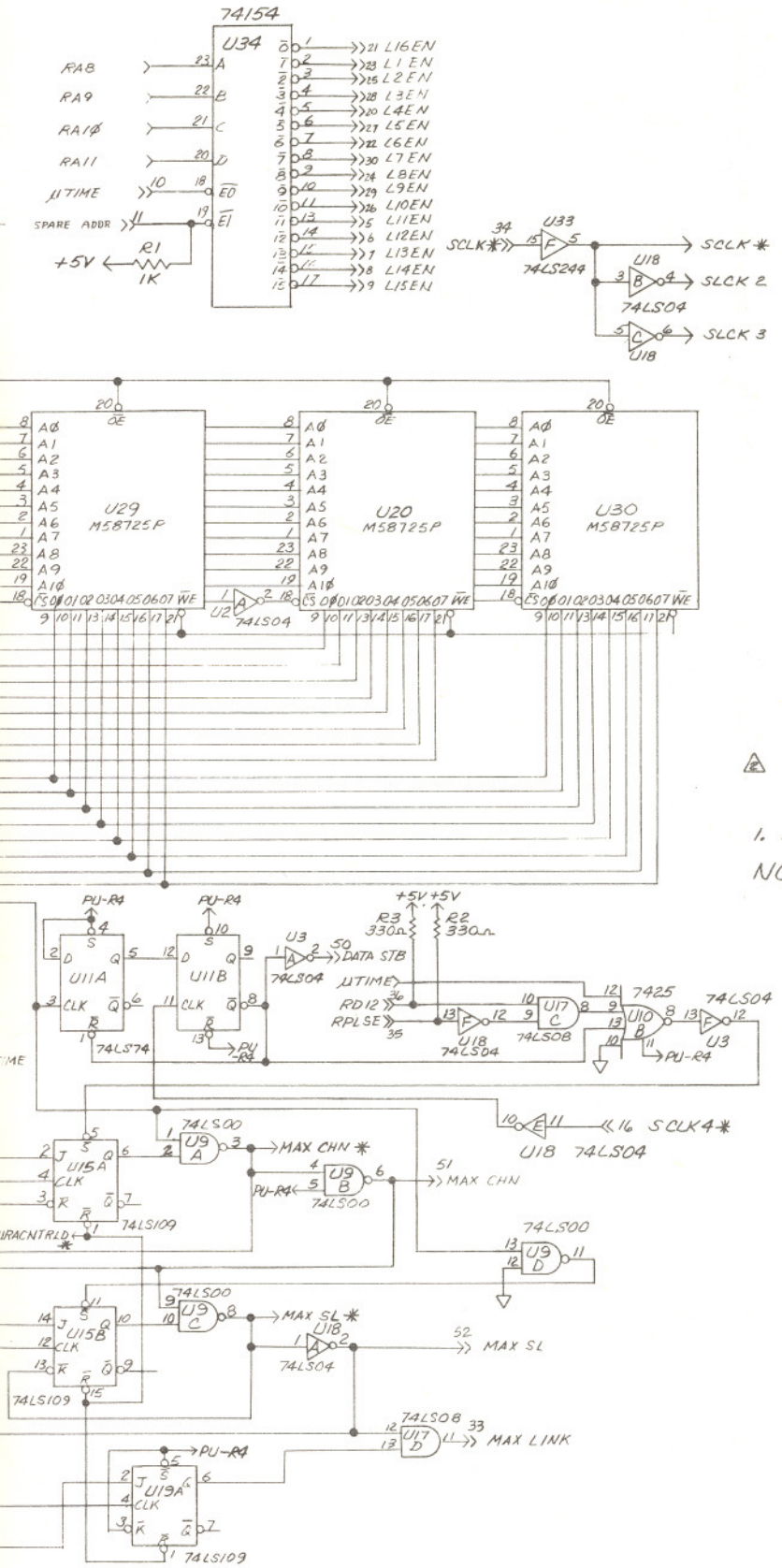
Figure 5-4. CS348-Q1 Control Sequencer Card, Schematic Diagram.


SPARE
+5VDC
GND
+5V
PU-R4
SCLK 3
SCLK2
74LS244
74LS161
74LS157
74LS189
74LS163
74LS74
74LS00
74LS04
74LS08
74LS32
74LS109
M58725P
7425
INS820
R4 1K


74154
U34
RA8
RA9
RA10
RA11
μTIME
SPARE ADDR
+5V
R1
1K
PU-R4
μPMWE*
SCLK*
U25
74LS74
μPMOE*
U21
U29
U20
U30
M58725P
74LS04
74LS244
74LS189
74LS163
74LS157
74LS161
74LS109
74LS00
74LS08
74LS32
74LS74
μOUT STB
SCLK2
μCHN
μRACNTRLD*
MAX CHN*
(RPD12*)
MAX SL*
μAC
DATA STB
RPLSE
RD12
R3 330Ω
R2 330Ω
7425
SCLK4*
MAX CHN
MAX SL
MAX LINK
RA0
RA1
RA2
RA3
MAX TIME
RA4
RA5
RA6
RA7
RA8
RA9
RA10
RA11

10307

REVISIONS			
SYM	DESCRIPTION	DATE	APPROVED



⚠ ALL 0.1µF CAPACITORS TO BE INSTALLED BETWEEN +5V AND GND, IN CLOSE PROXIMITY TO INTEGRATED CIRCUITS.

1. ALL RESISTOR VALUES ARE IN OHMS ±5%, 1/4W.

NOTES: UNLESS OTHERWISE SPECIFIED

INTEGRATED CIRCUIT CHART			
REF DES	TYPE	Vcc	GND
U34	74154	24	12
U15, U19	74LS109	16	8
U11, U25	74LS74	14	7
U24, U33	74LS244	20	10
U20, U21, U29, U30	M58725P	24	12
U26	74LS32	14	7
U17	74LS08	14	7
U22, U27, U31	74LS157	16	8
U12, U13, U14	74LS163	16	8
U6, U7, U8	74LS189	16	8
U5, U9	74LS00	14	7
U1, U2, U3, U18	74LS04	14	7
U10	7425	14	7
U4, U16, U23, U28, U32	74LS161	16	8

Figure 5-5. AG351-Q1 Address Generator Card, Schematic Diagram.

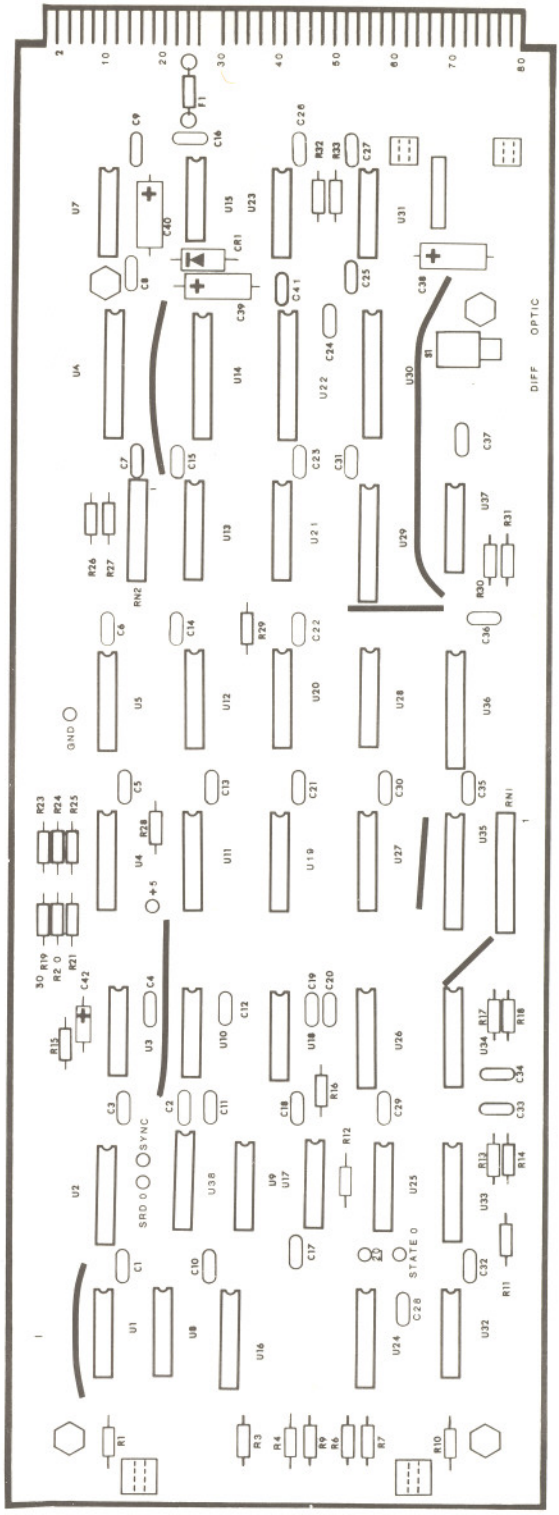


Figure 5-6. DR317-Q1 Receiver Input Card A.

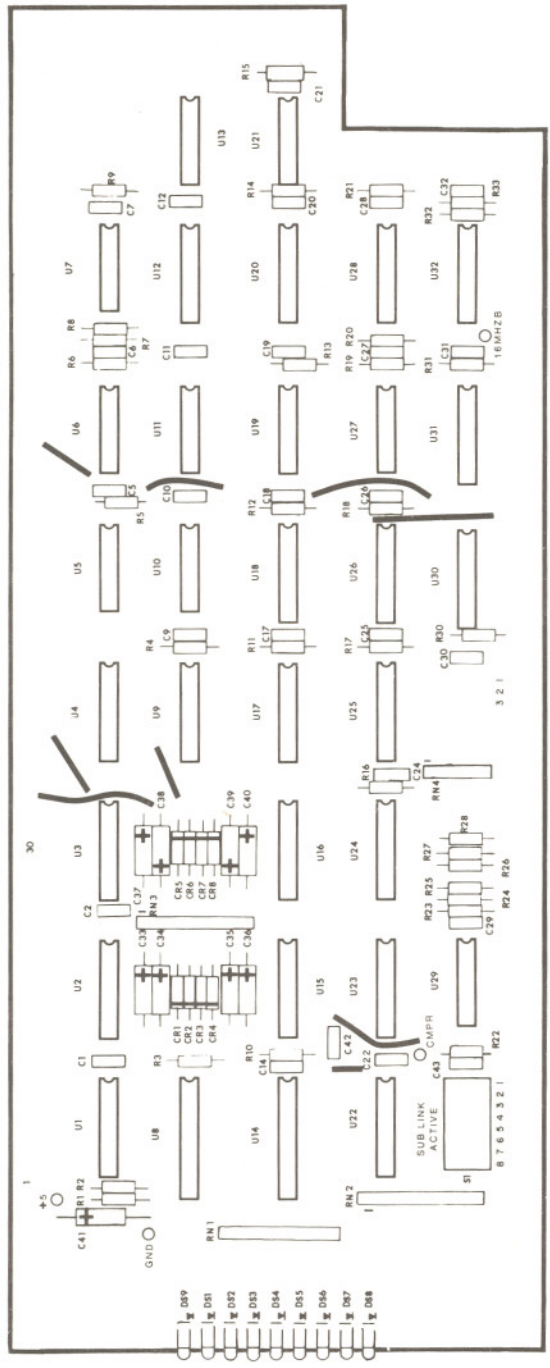


Figure 5-7. DR317-Q1 Receiver Input Card B.

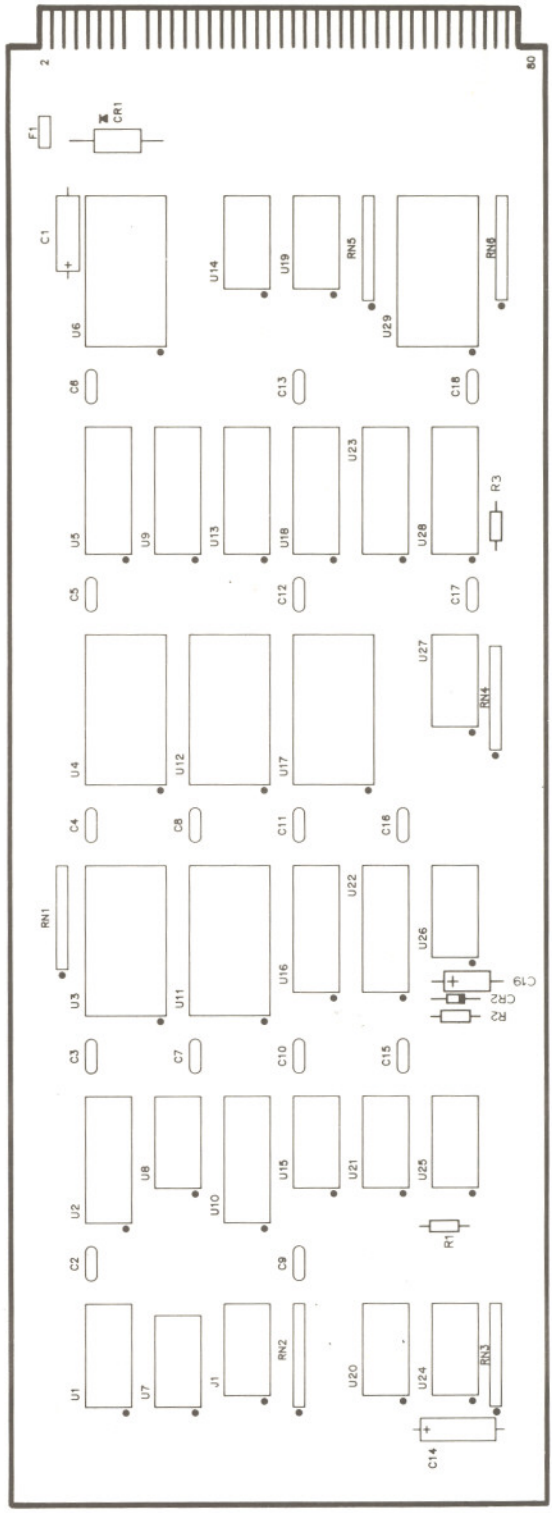


Figure 5-8. CS348-Q1 Control Sequencer Circuit Board Assembly.

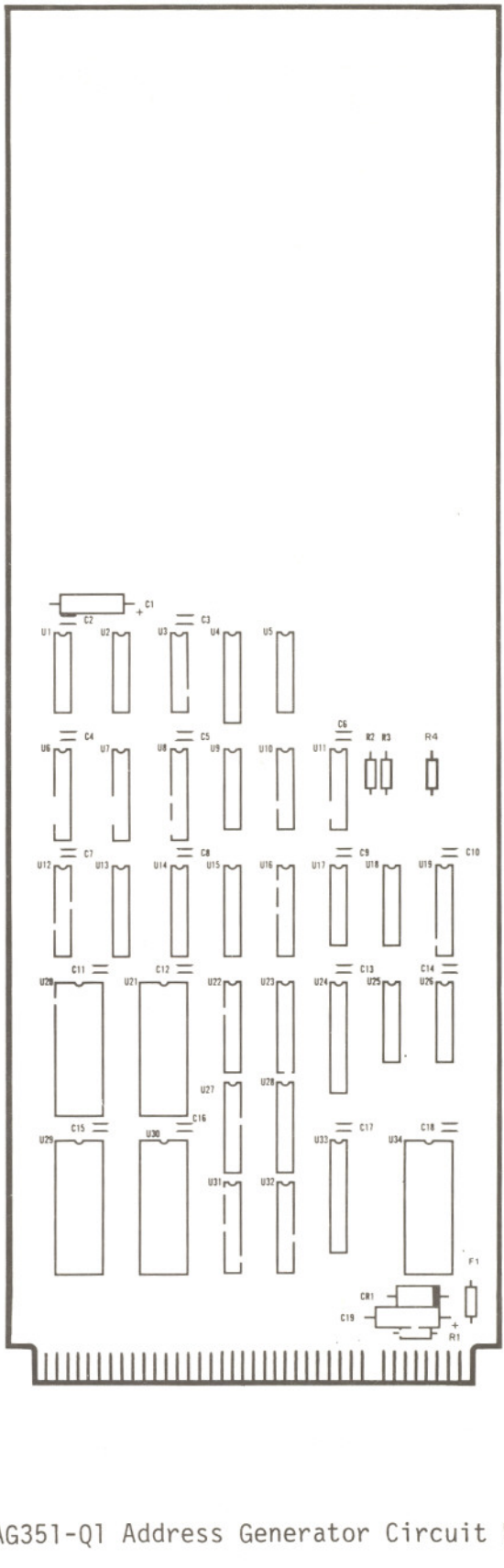


Figure 5-9. AG351-Q1 Address Generator Circuit Board Assembly.

SECTION VI
REPLACEMENT PARTS

6-1. GENERAL.

The MC312-Q1 Master Receiver Case features modular construction throughout, making maximum use of plug-in assemblies for ease of installation and maintenance. The component parts, processes and assembly details have been carefully selected and tested to produce end items capable of meeting the operating performance and reliability goals established for the MR312-Q1 and for the HD310 System, of which it is a part.

6-2. To this end, the list of recommended parts to be inventoried by using facilities in support of this equipment includes the board-level assemblies and mechanical subassemblies capable of field replacement without the need for specialized tools and equipment, and which will maintain the demonstrated reliability and performance required for the system.

6-3. REPLACEMENT PARTS LIST.

The following numbers are recommended for stocking in support of the MR312-Q1 Master Receiver:

PART NUMBER	DESCRIPTION	QTY USED PER ASSY
Q10065	MR312-Q1 Master Receiver without Power Supply, plug-in modules or cards	1
DR317-Q1	Receiver Input Cards	1-16
CS348-Q1	Control Sequencer Card	1
AG351-Q1	Address Generator	1
DD354-Q1	Differential Driver Card	1*
DD355-Q1	Differential Receiver Card	1**
CI356-Q1	Computer Interface Card	1
PS320-Q1	Power Supply Module	1

PART NUMBER	DESCRIPTION	QTY USED PER ASSY
TG319-Q1	Time Code Generator	1
RC321	Tape Control Module (Optional)	1 (opt)
DA313-Q1	Digital-to-Analog Converter Module (Optional)	1 (opt)
PT06A-12-3S	Three-pin Bendix Connector (J417)	1
PT06A-8-4P	Four-pin Bendix Connector (J401-J416)	1-16
AMP 205209-1	Subminiature Rect. Connector (J418, 419 and 421)	3
AMP 205210-1	Subminiature Rect. Connector (J422)	1
AMP 205212-1	50-pin Subminiature Plug (J423 and 425) Q11034	2
AMP 205211-1	Subminiature Rect. Connector Q11035 (J420, 424 and 426)	3

* Two if a remote Digital-to-Analog Converter is used. A DD354-1-Q1 (long) card is used if an RC321 Tape Control Module is NOT used and a DD354-2-Q1 (short) card is used if an RC321 Tape Control Module IS used in the system.

** A DR355-1-Q1 (long) card is used if an RC321 Tape Control Module is NOT used and a DR355-2-Q1 (short) card is used if an RC321 Module IS used in the System.

6-4. RECOMMENDED STOCKING LEVELS.

A rational stocking program should be based on the total number of each item of equipment to be used in the installation; e.g. the total number of MR312-Q1 Master Receivers and, from the list, the total number of subsidiary parts and assemblies. On this basis, the recommended stocking level is 5% of the total quantity of each item, or a quantity of one, whichever is greater.

APPENDIX A

RECEIVER PROGRAMMER/REMOTE COMPUTER INTERFACE FORMAT

1-1. GENERAL.

There are three major groups of commands that can be specified by the remote computer to direct the receiver programmer's output format. Group A commands reset the programmer and terminate the execution of the current command. Group B commands are preceded by a Group A command They are stored in the receiver programmer's plan memory for execution at a later time. Group C commands are used for access and control of the Digital-to-Analog Converters, Time Code Generator and Recorder and do not interfere with data transmission for the computer.

1-2. In addition to the commands from the remote computer, there are start and stop control flags from the real time clock that can modify the programmer's operation when turned on.

2-1. COMPUTER GENERATED COMMANDS TO RECEIVER PROGRAMMER.

2-2. Group A.

A. RDI, A READ DIRECT.

Number of words = 2

The command directs the programmer to execute the next word as an instruction.

A = 0 Read Live data

A = 1 Read Recorded data

B. RDR, A, P READ, PLAN.

Number of words = 1

Start execution of the plan specified by P. P is set up to accept sixteen plans, P = 0 thru 15.

Example: RDR,0,3 Execute plan 3 with live data immediately, use internal clock.

C. DMP, A ALL CHANNEL READ.

0	0	1	0	1	0	1	0	0	A	0	0	0	0	0	0

Number of words = 1

Output all active channels to the remote computer.

A = 0 Read Live data

A = 1 Read Recorded data

Example: DMP, 4 Read Live data for all active channels to the remote computer when the Real time clock equals to the content of the Start time register. Use internal clock.

D. LPN, P LOAD PLAN.

0	0	1	0	1	1	0	0	0	0	0	0	P (4)

Number of words ≤ 4096.

Start filling the plan memory with the Group B type instructions.

Plan number is specified by P.

P = 0 to 15

```
Example:   LPN,3      Start loading plan 3
           TME,0
           CHN,1,2,3
             .
             .
             .
           GROUP B Instruction      } Operation Instruction
             .
             .
             .
           EPN        End of plan.
```

2-3. Group B.

A. CHN,L,S,C READ CHANNEL.

Read a single channel data.

Example:

CHN,5,2,1 Read Channel 5 at sub-link 2 and link 1.

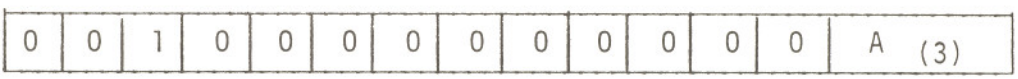
B. LNK,L READ LINK.

Read a set of link data, specified by L.

Example:

LNK, 4 Read a set of link 4 data.

C. TME, A READ TCG.



Read information specified by A to the remote computer.

A = 0 millisec.
A = 1 sec, min.
A = 2 hour, day.
A = 3 month, year.
A = 4 serial number
A = 5 footage count.
A = 6 unused.
A = 7 unused.

D. EPN END OF PLAN

0	0	1	0	0	0	1	0	0	0	0	0	0	0	0	0

This is an end of plan marker. This statement should be the last statement of every plan.

Example:

```
LPN,3     Start load plan 3
TME,0
   .
   .
GROUP B Instructions
   .
   .
   .
EPN       End of plan.
```

?-4. Group C.

A. SLA,C,M SEL D/A CHANNEL.

0	1	0	0	0	0	0	1	1	C 4	M 3

Number of words = 2

Select the D/A channel. This command sets up the D/A channel pointer so that the second command, the STA type command, can direct the selected channel data flow.

C = Module case number

M = Module number within a module case

Example:

```
SLA, 5, 6   Set up pointer to module case 5, module 6. Wait
            for STA command to direct data flow to the indi-
            cated A/D channel.
```

B. STA,L,S,C SET D/A CHANNEL DATA FLOW.

0	1	0	1	L 4	S 3	C 5

Direct the D/A module selected by the previous SLA command to display the analog channel specified by L,S, and C fields. This STA command will be replaced by the later STA as long as the D/A channel pointer remains the same.

L = Link address

S = Sub-link address

C = Channel address

Example:

STA, 1, 2, 3 Direct the selected D/A channel to display Channel 3, Sub-link 2, Link 1 sampled data.

C. SCK,A,D SET REAL TIME CLOCK.

1	0	A (2)	D_2 (12)

Number of words = 1

Load real time clock register with D.

D_2 is the data field in binary format.

A = 0 D =

Minutes (6)	Seconds (6)

A = 1 D =

0	0	Day (5)	Hours (5)

A = 2 D =

X	Year (7)	Month (4)

X = Don't Ca

Example:

SCK,1,1521 Load day 15 and 21 hours in real time clock

D. STM,A,D, SET TIMER.

1	1	$A_{(2)}$	D_2

Number of words - 1

Load start time or duration with register D.

D_2 is the data field in binary format.

A = 0 D =

Start Minutes (6)	Start Seconds (6)

A = 1 D =

0	0	0	0	0	0	0	Start Hours (5)

A = 2 D =

Duration Minutes (6)	Duration Seconds (6)

A = 3 D =

0	0	0	0	0	0	0	Duration Hours (5)

Example:

STM,0,3605 Load start time or 36 minutes and 5 seconds.

E. PCM,A,P SET PCM CONTROL AND CLOCK.

1	0	1	1	0	$A_{(3)}$	P (8)

Number of words = 1

A = Relative playback tape speed to the original recording.

A = 0 Same speed
A = 1 One-half speed
A = 2 One-quarter speed
A = 3 One-eighth speed
A = 4 One-sixteenth speed

A = Relative playback (continued)

A = 5 ~~External clock~~ NOT USED

A = 6 Not used

A = 7 Not used

P = Digital tape recorder control

P_0 = 1 = Record

P_1 = 1 = Fast

P_2 = 1 = Reverse

P_3 = 1 = Forward

P_4 = 1 = Stop

P_5 = Unused

P_6 = Unused

P_7 = Unused

Example:

PCM, 0, 0 Playback tape at original recording rate.

3-1. RECEIVER PROGRAMMER GENERATED DATA WORDS TO COMPUTER

3-2. Channel Data.

A	B	C	D	DATA (12)

A = 1 START OF SCAN

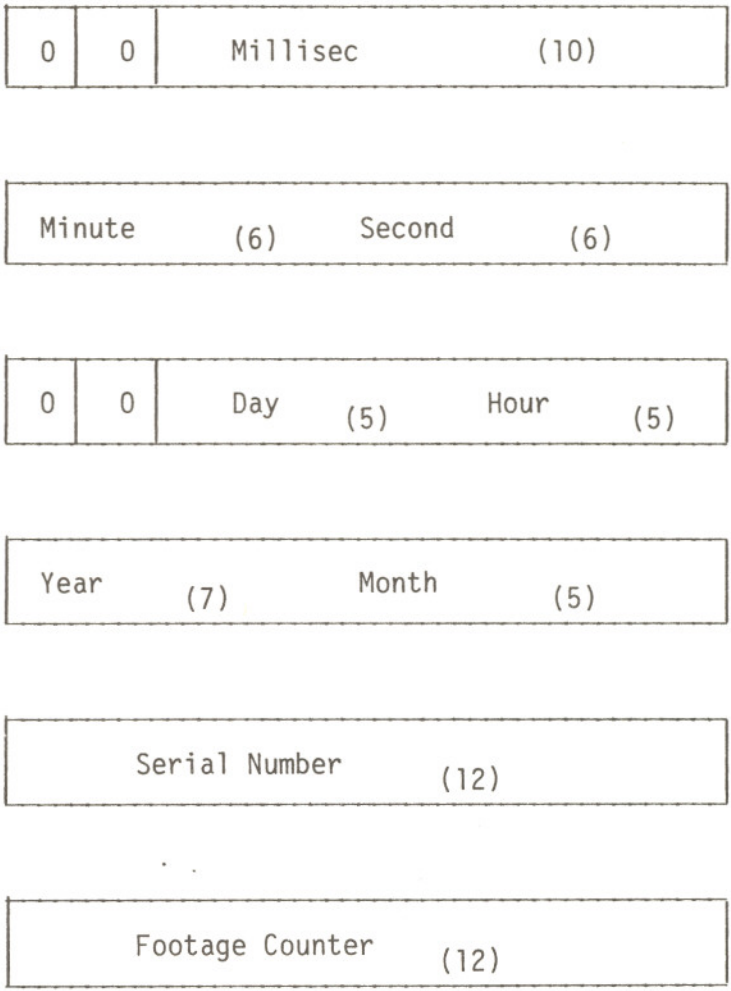
B = 1 START OF LINK

C = 1 START OF SUB-LINK

D = 1 ERROR (LINK OR SUB-LINK)

3-3. Time or Miscellaneous data.

X	X	X	X	DATA (12)

3-3. Time or Miscellaneous Data (continued)

Possible Output Data Words.